# MAQ®20

## Industrial Data Acquisition and Control System

## MA1046

## MAQ20-BRDG1
## Hardware User Manual


DATAFORTH®

**MAQ20-BRDG1 Hardware User Manual**
**MA1046 Rev. D – March 2024**

**ISO9001:2015-Registered QMS**

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## About Dataforth Corporation

"Our passion at Dataforth Corporation is designing, manufacturing, and marketing the best possible signal conditioning, data acquisition, and data communication products. Our mission is to set new standards of product quality, performance, and customer service." Dataforth Corporation, with more than a quarter century of experience, is the worldwide leader in Instrument Class® Industrial Electronics – rugged, high performance signal conditioning, data acquisition, and data communication products that play a vital role in maintaining the integrity of industrial automation, data acquisition, and quality assurance systems. Our products directly connect to most industrial sensors and protect valuable measurement and control signals and equipment from the dangerous and degrading effects of noise, transient power surges, internal ground loops, and other hazards present in industrial environments.

Dataforth spans the globe with more than 50 International Distributors and US Representative Companies. Our customers benefit from a team of over 130 salespeople highly trained in the application of precision products for industrial markets. In addition, we have a team of application engineers in our Tucson factory ready to solve any in-depth application questions. Upon receipt of an RFQ or order, our Customer Service Department provides fast one-day delivery information turnaround. We maintain an ample inventory that allows small quantity orders to be shipped from stock.

Dataforth operates under an ISO9001:2015 quality management system.

## Contacting Dataforth Corporation

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## Errata Sheets

Refer to the Technical Support area of Dataforth's website (www.dataforth.com) for any errata information on this product.

## 1.0 System Features

The MAQ20 Data Acquisition System encompasses more than 35 years of design excellence in the process control industry. It is a family of high performance, DIN rail mounted, programmable, multi-channel, industrially rugged signal conditioning I/O and communications modules.

**Instrument Class Performance**

- ±0.035% Accuracy
- Industry leading ±0.3°C CJC Accuracy over full operating temperature range
- Ultra-low Zero and Span Tempco
- Over-range on one channel does not affect other channels
- 1500Vrms Channel-to-Bus Isolation
- 240Vrms Continuous Field I/O Protection
- ANSI/IEEE C37.90.1 Transient Protection
- Ventilated Communications and I/O Modules
- Industrial Operating Temperature of -40°C to +85°C
- Wide Range 7-34VDC Power
- CE Compliant
- UL/cUL (Class I, Div 2, Groups A, B, C, D) Compliant, file E232858
- ATEX Compliance pending

**Industry Leading Functionality**

- The system is a Modbus Server and can be operated remotely with no local PC
- Up to 8GB of logged data can be transferred via FTP during real-time acquisition
- Up to 24 I/O modules, or 384 analog or 480 digital channels, per system, 19” rack width
- Per-channel configurable for range, alarms, and other functions
- Backbone mounts within DIN rail and distributes power and communications
- System firmware automatically registers the installation and removal of I/O modules
- I/O modules can be mounted remotely from the Communications Module
- Equal load sharing power supply modules allow for system expansion
- Hot Swappable I/O modules with Field-side pluggable terminal blocks on most models
- Sophisticated package enables high density mounting in 3U increments
- DIN Rail can be mounted on a continuous flat panel or plate

**Distributed Processing Enables Even More Functionality**

- Output modules are programmable for user-defined waveforms
- Discrete I/O modules have seven high level functions:
  - Pulse Counter
  - Frequency Counter
  - Waveform Measurement
  - Time Between Events
  - Frequency Generator
  - PWM Generator
  - One-Shot Pulse Generator

**Multiple Software Options**

- Free Configuration Software
  - ReDAQ Shape Graphical HMI Design & Runtime Solution
- Intuitive Graphical Control Software
  - ReDAQ Shape Graphical HMI Design & Runtime Solution
  - Phyton API
  - OPC Server
  - Programming examples and LabVIEW Vis

## 2.0 System Description and Documentation

A MAQ20 Data Acquisition System must have as a minimum a Communications Module, a Backbone, and one I/O Module. Examples include:

- MAQ20-COMx Communications Module with Ethernet, USB and RS-232 or RS-485 Interface
- MAQ20-DIOx Discrete Input / Output Module
- MAQ20-xTC Type x Thermocouple Input Module
- MAQ20-mVxN, -VxN Voltage Input Module
- MAQ20-IxN Process Current Input Module
- MAQ20-IO, -VO Process Current Output and Process Voltage Output Module
- MAQ20-BKPLx x Channel System Backbone

Refer to https://www.dataforth.com/maq20 for a complete listing of available modules and accessories.

System power is connected to the Communications Module, which in turn powers the I/O modules. For systems with power supply requirements exceeding what the Communications Module can provide, the MAQ20-PWR3 Load Share Power Supply module is used to provide additional power. When a MAQ20 I/O module is inserted into a system, module registration occurs automatically, data acquisition starts, and data is stored locally in the module. The system is based on a Modbus compatible memory map for easy access to acquired data, configuration settings, and alarm limits. Information is stored in consistent locations in module memory for ease of use and system design.

MAQ20 modules are designed for installation in Class I, Division 2 hazardous locations and have a high level of immunity to environmental noise commonly present in heavy industrial environments.

**The MAQ20 strain gage input module, MAQ20-BRDG1**, has 4 input channels and can interface to full, half, and quarter bridge sensors using 4-wire or 6-wire connections. All channels are individually configurable for range, alarms, and averaging to match the most demanding applications. In addition, sampling rate, resolution, bandwidth, excitation voltage, and shunt calibration are user settable parameters. High, Low, High-High and Low-Low alarms provide essential monitoring and warning functions to ensure optimum process flow and fail-safe applications. Hardware low-pass filtering in each channel provides rejection of unwanted frequencies. Field connections are made through high density spring cage terminal blocks with positions designated for the termination of wiring shields.

Input-to-Bus isolation is a robust 1500Vrms and each individual channel is protected up to 30Vrms continuous overload in the case of inadvertent wiring errors. Overloaded channels do not adversely affect other channels in the module which preserves data integrity.

For details on installation, configuration, and system operation, refer to the manuals and software available for download from www.dataforth.com. This includes, but is not limited to:

MA1036 MAQ®20 Quick Start Guide

MA1040 MAQ®20 Communications Module Hardware User Manual

MA1038 MAQ®20 ReDAQ Shape for MAQ®20 User Manual

MA1064 MAQ®20 MAQ20 Python API User Manual

MAQ20-940 ReDAQ Shape Software for MAQ®20 – Developer Version

MAQ20-941 ReDAQ Shape Software for MAQ®20 – User Version

MAQ20-945 MAQ®20 Configuration Software Tool

MAQ20-960 MAQ20 Python API

## 3.0 Specifications

| **STRAIN GAGE INPUT MODULE** | Typical at $T_A$ = +25°C and +24V system power |
|---|---|
| **Model Number, Sensor Type & Input Range**<br>MAQ20-BRDG1 | Full, Half, Quarter Bridge (with external bridge completion)<br>4-wire or 6-wire connection |
| **Number of Channels** | 4 |
| **Per Channel Setup** | Individually configurable for range, alarms, averaging |
| **Input Range** | +/-100mV at 0.8mV/V to 40mV/V Sensitivity |
| **Input Protection** | |
| Continuous | 30Vrms max |
| Transient | ANSI/IEEE C37.90.1 |
| **Excitation Voltage** | 2.5V, 3.3V, 5.0V, 10.0V @ 80mA max |
| **Bridge Resistance** | 100ohm to 1kohm |
| **Shunt Calibration** | 60kohm, 100kohm, 200kohm, External |
| **Excitation Protection** | |
| Continuous | 30Vrms max |
| Transient | ANSI/IEEE C37.90.1 |
| **CMV** | |
| Channel-to-Bus | 1500Vrms, 1 min |
| Channel-to-Channel | ±3V peak |
| Transient | ANSI/IEEE C37.90.1 |
| **CMR** | 100dB @ 50/60 Hz |
| **NMR** | 60dB/decade |
| **Accuracy(1)** | ±0.03% span |
| **Linearity** | ±0.01% span |
| **Resolution** | 0.0005% to 0.005% span |
| **ADC Resolution** | 24-bit |
| **Stability** | |
| Zero | 50ppm/C |
| Span | 75ppm/C |
| **Bandwidth** | Programmable to 17kHz |
| **Sampling Rate, Simultaneous** | 1kS/s to 32kS/s burst |
| **Alarms** | High / High-High / Low / Low-Low |
| **Power Supply Current** | 400mA |
| **Dimensions (h)(w)(d)** | 4.51” x 0.60” x 3.26” (114.6mm x 15.3mm x 8.28mm) |
| **Environmental** | |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -40°C to +85°C |
| Relative Humidity | 0 to 95%, non-condensing |
| **Emissions, EN61000-6-4** | ISM Group 1 |
| Radiated, Conducted | Class A |
| **Immunity EN61000-6-2** | ISM Group 1 |
| RF | Performance A +/- 0.5% Span Error |
| ESD, EFT | Performance B |
| Certifications | Heavy Industrial CE<br>UL/cUL (Class I, Div 2, Groups A, B, C, D) file E232858<br>ATEX Pending |

(1) Includes linearity/conformity, hysteresis, and repeatability.

## 4.0 Unpacking

Each MAQ20 Data Acquisition System component is shipped in electro-static discharge (ESD) protective packaging. Use appropriate ESD protection measures while unpacking. Check visually for physical damage. If physical damage is noted, file a claim with the shipping carrier and contact the factory.

## 5.0 Module Dimensions and I/O Connections

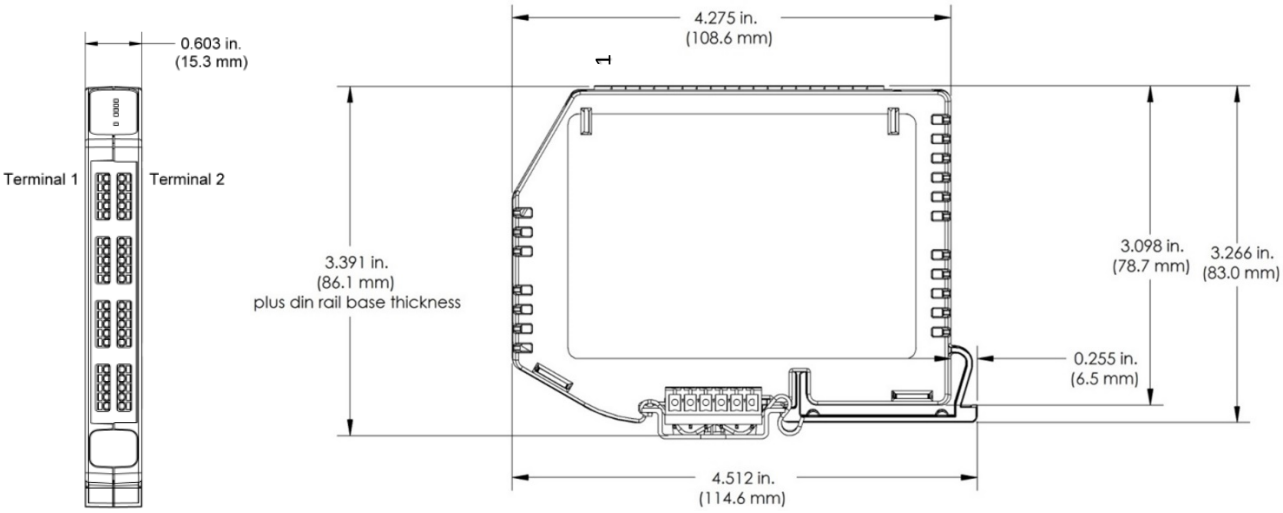
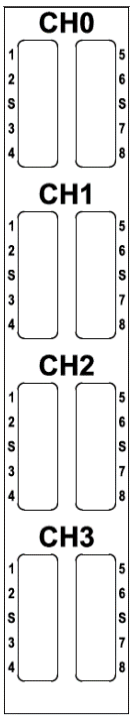



**Figure 1: Module Dimensions**

**Table 1: MAQ20-BRDG1 Input Terminal Block Connections**




| | FIELD CONNECTION | TERMINAL | TERMINAL | FIELD CONNECTION |
|---|---|---|---|---|
| CHANNEL 0 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |
| CHANNEL 1 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |
| CHANNEL 2 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |
| CHANNEL 3 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |

The high-density spring cage terminal blocks can accept the following wire sizes:

- Solid Wire AWG 26 to AWG 20
- Stranded Wire AWG 24 to AWG 20

MAQ20-BRDG1 modules and MAQ20 systems which contain MAQ20-BRDG1 modules are shipped with an accessory screwdriver which is used for sensor wire insertion and removal. If this screwdriver is not available, contact the factory for purchase, or use any screwdriver or slotted driver with 1/16” (1.6mm) tip.

**Sensor Wire Connection**

- Insert the slotted driver in the rectangular opening adjacent to the wire hole.
- Ensure the driver is perpendicular to the terminal block.
- Press the driver firmly into the opening.
- While holding the driver in place, insert the sensor solid or stranded wire into the round opening.
- Hold the sensor wire in place and remove the driver.
- Pull on the sensor wire to ensure it was captured.

**Figure 2: Sensor Wire Connection and Removal**

**Sensor Wire Removal**

- Insert the slotted driver in the rectangular opening adjacent to the wire hole.
- Ensure the driver is perpendicular to the terminal block.
- Press the driver firmly into the opening.
- While holding the driver in place, pull the sensor solid or stranded wire out of the round opening.
- Remove the driver.

## 6.0 Module Installation and Removal

The MAQ20 I/O module package has been designed for easy insertion into and removal from a system and can mate with DIN rails mounted flush on continuous panels or plates.

To install a module:

1. Orient the module with the field connector facing out.
2. Align the angled surface on the top rear corner with panel or plate the DIN rail is mounted to.
3. Slide the module down to capture the DIN rail with the hook on the module.
4. Rotate the module and snap in place.

To remove a module, reverse the steps in the installation process. If space is available, the clip at the bottom of the module can be squeezed by hand to release. For tight installations, insert a flat blade screwdriver into the recess in the clip (5), place the shaft of the screwdriver against the curved part of the clip and gently pry the clip to release (6) as shown below.

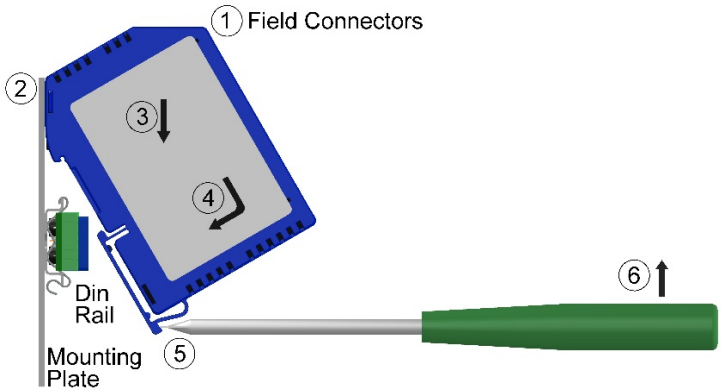



**Figure 3: Module Installation and Removal**

Multiple rows of MAQ20 modules can be mounted at a 3U vertical spacing interval. Backbones can be combined to add I/O modules to a system. A system is only allowed to have one MAQ20-COMx module. Some possible configurations in a 19” rack are shown below.

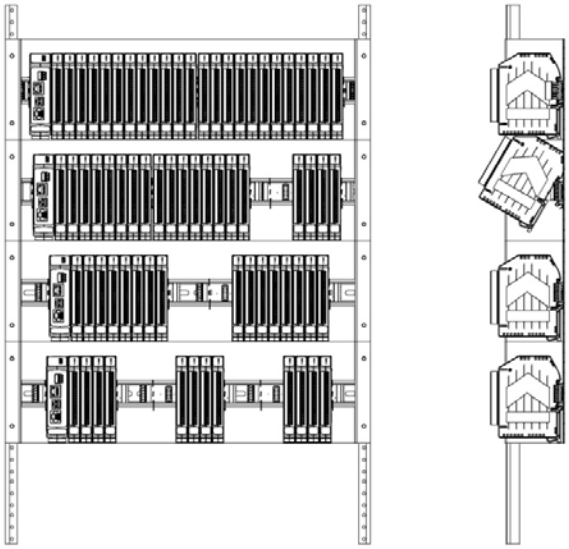


**Figure 4: Possible System Configurations**

## 7.0 LED Indicators

A set of 5 LEDs on the top panel of the MAQ20 I/O modules indicate module power, operation, communication, and alarm status.


**Figure 5: LED Indicators**

**LED Function and Troubleshooting Tips:**

**PWR**

Normal operation: BLUE, solid lit

LED Off: Abnormal power situation

- Verify that a MAQ20-COMx is present in the system.
- Verify that the MAQ20-COMx module has 7-34VDC power connected and turned on
- Determine if the module is communicating by observing the TX and RX LEDs

**STAT**

Normal operation: GREEN, 1 Hz blinking

Module Detect: A write to the Module Detect Register will force this LED to blink at 5Hz rate for 5 seconds so the module location in a system can be visually identified. Referring to the Address Map, this module register is at address 98, offset from the module base address.

LED Constant On or Constant Off: Abnormal operation

- Remove and reinstall module to force a reset.
- Remove and reinstall module into another backbone position.
- Determine if the module is communicating by observing the TX and RX LEDs.

**RX, TX**

Normal Operation – YELLOW, rapid blinking during communication with MAQ20-COMx module

LED Constant Off: Abnormal operation or no communications to MAQ20-COMx module

- Verify communications by sending a request for data. Note that the fast communications rate used on the system backbone will result in the LED appearing dim due to short blinking cycle.
- Verify that the PWR and STAT LED indicate normal operation.
- Verify that there is only one MAQ20-COMx module installed in the system.

**ALM**

Normal operation: Off

Alarm Condition Detected: RED, solid lit.

- One or more alarms have been tripped.
- Read module Alarm Registers based on Alarm Configuration to determine system status.

The following troubleshooting tips can be used to further diagnose and fix system problems:

- Remove and reinstall MAQ20 I/O module and/or MAQ20-COMx module to verify proper insertion into Backbone.
- Remove and reinstall MAQ20 I/O module into another backbone position.
- If a Backbone extension cable is used, ensure that the connections are made correctly.

## 8.0 Module Identification and Status Registers

Module identification including model number, serial number, date code and firmware revision are stored in module registers starting at address 0.

I/O modules in a system are identified in general by their model number (MAQ20-BRDG1, MAQ20-VDN, etc.) and uniquely by their Serial Number printed on the side label (1234567-89). When I/O modules are installed in the system, only a general identifier is visible on the front of the module (BRDG, V, etc.). Wire tags or additional labeling applied to the module terminal block may be used for visible unique identification in an installed system. Additionally, the system has a utility to provide a visual indication of module response for identification. Any write to address 98 plus the offset based on the Registration Number will blink the STATUS LED on the top angled surface of the module at a 5Hz rate for 5 seconds.

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Module identification is stored starting at module register address 0, which is system register address 2000 * R + 100, where R is the module Registration Number. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

**Table 2: MAQ20-BRDG1 Address Map Excerpt – Module Information**

| Address Range 0 - 99: Module Information | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 0 | R | 15 | Device Description | MAQ20-BRDG1 | Characters, Numbers, "-" and Space | ASCII |
| 19 | R | 11 | Serial Number | S1234567-89 | Characters, Numbers, "-" and Space | ASCII |
| 30 | R | 5 | Date Code | D0915 (D<week><year>) | Characters, Numbers | ASCII |
| 35 | R | 5 | Firmware Rev | F1.00 | Characters, 0-9 and "." | ASCII |
| 40 | R | 1 | Input Channels | 8 Input Channels | 8 | ASCII |
| 41 | R | 1 | Output Channels | 0 Output Channels | 0 | ASCII |
| 98 | W | 1 | Module Detect | Any write will blink Status LED at 5Hz for 5 seconds | 0 to 65,535 | INT16 |

For troubleshooting purposes, reset status, communications errors, and invalid data written to a module are monitored and made available to the user. Module diagnostic registers starting at module register address 1900 hold this information.

**Table 3: MAQ20-BRDG1 Address Map Excerpt – Status Registers**

| Address Range 1900 - 1999: Status Registers | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Type** | **Example** | **Range** | **Data type** |
| 1900 | R/W | 1 | Watchdog Reset | 0 = Normal<br>1 = Watchdog Reset Occurred | 0 or 1 | INT16 |
| 1902 | R/W | 1 | I2C Error | I2C TX Error Counter | 0 to 65,535 | INT16 |
| 1903 | R/W | 1 | I2C Error | I2C RX Error Counter | 0 to 65,535 | INT16 |
| 1906 | R/W | 1 | Numeric Error | Increments when a value received is outside of the allowed range.<br>Default = 0. | 0 to 65,535 | INT16 |
| 1908 | R/W | 1 | UART RX Error | UART RX Error Counter Command Too Short<br>Default = 0 | 0 to 65,535 | INT16 |
| 1909 | R/W | 1 | UART RX Error | UART RX Error Counter Command Too Long<br>Default = 0 | 0 to 65,535 | INT16 |
| 1910 | R/W | 1 | UART RX Error | UART RX Error Counter Command received in invalid state.<br>Default = 0 | 0 to 65,535 | INT16 |

## 9.0 Building a System

An automated I/O module registration process reduces system setup to three basic steps:

**STANDARD SETUP PROCESS**

1.) Install a MAQ20-BKPLx backbone in a DIN rail then insert a MAQ20-COMx module in the left-most position and apply power.

2.) Install any MAQ20 I/O Module in any vacant local or remote backbone position. Observe that the green Power LED is on and communications activity is seen on the TX and RX LEDs. Allow 1 second for registration. This module has now been assigned Registration Number 1.

Label and connect field wiring to the I/O Module. If desired, record module physical position in the system.

3.) Repeat Step 2 for all remaining MAQ20 I/O modules in the system. Subsequent modules installed are assigned Registration Number 2, 3, etc., allowing 1 second for registration. The Registration Number sequence matches the physical sequence of module installation.

**ALTERNATE SETUP PROCESS**

1.) Do not apply power. Install a MAQ20-BKPLx backbone in a DIN rail then insert a MAQ20-COMx module in the left-most position and install all required MAQ20 I/O modules in any vacant local or remote backbone position. Label and connect field wiring to the I/O Module and if desired record physical position in the system.

2.) Apply system power and observe that each module has the green Power LED on and communications activity is seen on the TX and RX LEDs. Registration is complete when module TX and RX LEDs all have a repeating blink pattern. All modules have now been assigned Registration Numbers, but in a random sequence not associated with the physical position on the backbone.

**NOTES:**

Once the registration process is complete, Registration Numbers are permanent as long as I/O modules are not removed from or added to a system. When system power is cycled or the system is reset, I/O module Registration Numbers will always remain the same. If I/O modules are removed while the system is powered, they will be unregistered, and the slots or registration numbers become available to register new modules once inserted. If I/O modules are removed while the system is powered and then the power is cycled, the remaining modules will remain registered with their originally assigned Registration Numbers.

I/O modules in a system are identified in general by their model number (MAQ20-RTD31, MAQ20-VDN, etc.) and uniquely by their Serial Number printed on the side label (i.e. 1234567-89). When I/O modules are

installed in the system, only a general identifier is visible on the front of the module (RTD, V, TC, etc.). Wire tags or additional labeling applied to the module terminal block may be used for visible unique identification in an installed system.

MAQ20-940 ReDAQ Shape Software for MAQ20 automatically assigns tag names to each input and output channel. These can be changed by the customer to associate channels with input wiring or parameters measured and controlled.

The system does not identify I/O modules by physical position on a backbone, only by registration sequence. MAQ20-940 ReDAQ Shape Software for MAQ20 provided by Dataforth shows a graphical representation of a system based on registration sequence and not by physical position. Tools within the software package allow the user to reassign and save Registration Numbers thereby making graphical representations match physical location for a single, local backbone and retain permanence. Refer to the MAQ20 I/O Module Registration section for further details.

Module Detect: A write to the Module Detect register at I/O module register address 98 plus the module offset based on Registration Number will blink the STAT LED on the top angled surface of the module at a 5Hz rate for 5 seconds so the module location in a system can be visually identified.

## 10.0 Maintaining a System

The MAQ20-COMx Communications Module periodically scans the system and will detect if a MAQ20 I/O module has been removed from the system or has lost communications. When this happens the module Registration Number will be released and available for reassignment.

Standard system maintenance involves a simple three step process:

**STANDARD MAINTENANCE PROCESS**

1.) Turn system power on and observe communications activity on the I/O modules.

2.) **CASE 1:** I/O module is replaced with one having a different model number or serial number: Remove a single MAQ20 I/O module from any local or remote backbone position. Replace the module with another having a different model number. This module can be installed in any vacant local or remote backbone position. Observe that the green Power LED is on and that there is communications activity on the TX and RX LEDs. Allow 1 second for registration. **This module now has the same Registration Number as the one removed.**

**CASE 2:** I/O module is suspected faulty and is to be replaced with the same model number: Remove a single MAQ20 I/O module from any local or remote backbone position. Replace the module with another of the same model number. This module can be installed in any vacant local or remote backbone position. Observe that the green Power LED is on and communications activity is seen on the TX and RX LEDs. Allow 1 second for registration. **This module now has the same Registration Number as the one removed.**

Label and connect input/output wiring to the I/O module and if desired record physical position in the system.

3.) Repeat Step 2 for any remaining MAQ20 I/O modules in the system requiring maintenance.

**ALTERNATE MAINTENANCE PROCESS**

1.) With the system power off, remove any I/O modules which are to be replaced. Replace the modules with others of the same or different model numbers. Modules can be installed in any vacant local or remote backbone position.

    Label and connect input/output wiring to the I/O module and if desired record physical position in the system.

2.) Apply system power and observe that each module has the green Power LED on and communications activity is seen on the TX and RX LEDs. Registration is complete when module TX and RX LEDs all have a repeating blink pattern. Replaced modules have now been assigned the Registration Numbers of those removed, but in a random sequence not associated with the physical position on the backbone. Modules which were not replaced retain their assigned Registration Numbers.

**NOTES:**

Once the registration process is complete, Registration Numbers are permanent as long as I/O modules are not removed from or added to a system. When system power is cycled or the system is reset, I/O module Registration Numbers will always remain the same. Tools within MAQ20-940 ReDAQ Shape Software for MAQ20 allow the user to reassign and save Registration Numbers. Refer to the MAQ20 I/O Module Registration section for further details.

Module Detect: A write to the Module Detect register at I/O module register address 98 plus the module offset based on Registration Number will blink the STAT LED on the top angled surface of the module at a 5Hz rate for 5 seconds so the module location in a system can be visually identified.

## 11.0 Expanding a System

The MAQ20-COMx Communications Module periodically scans the system and will detect if a MAQ20 I/O module has been added. When this happens the next available sequential Registration Number is assigned to the module.

Standard system expansion involves a simple three step process:

**STANDARD EXPANSION PROCESS**

1.) Turn system power on and observe communications activity on the I/O modules.

2.) Add a single MAQ20 I/O module in any local or remote backbone position. Observe that the green Power LED is on, and communications activity is seen on the TX and RX LEDs. Allow 1 second for registration. This module has now been assigned the next available sequential Registration Number.

Label and connect input/output wiring to the I/O module and if desired record physical position in the system.

3.) Repeat Step 2 for all remaining MAQ20 I/O modules to be added to the system. Subsequent modules installed are assigned the next sequential Registration Number.

**ALTERNATE EXPANSION PROCESS**

1.) With system power off, install all additional MAQ20 I/O modules in any vacant local or remote backbone positions. Label and connect field wiring to the I/O module and if desired record physical position in the system. Do not apply power.

2.) Apply system power and observe that each module has the green Power LED on and communications activity is seen on the TX and RX LEDs. Registration is complete when module TX and RX LEDs all have a repeating blink pattern. Added modules have now been assigned the next available sequential Registration Numbers, but in a random sequence not associated with the physical position on the backbone. Modules previously installed and registered in the system retain their assigned Registration Numbers.

**NOTES:**

Once the registration process is complete Registration Numbers are permanent as long as I/O modules are not removed from or added to a system. When system power is cycled or the system is reset, I/O module Registration Numbers will always remain the same. If I/O modules are removed while the system is powered, they will be unregistered, and the slots or registration numbers become available to register modules once inserted. If I/O modules are removed while the system is powered and then the power is cycled, the remaining modules will remain registered with their assigned Registration Numbers. Tools within MAQ20-940 ReDAQ Shape Software for MAQ20 allow the user to reassign and save Registration Numbers. Refer to the MAQ20 I/O Module Registration section for further details.

Module Detect: A write to the Module Detect register at I/O module register address 98 plus the module offset based on Registration Number will blink the STAT LED on the top angled surface of the module at a 5Hz rate for 5 seconds so the module location in a system can be visually identified.

## 12.0 MAQ20 I/O Module Registration and Reading Input and Excitation Signals

The MAQ20 Data Acquisition System uses an automated registration process which periodically scans the system and will detect when MAQ20 I/O modules are added and removed. Modules are assigned a sequential Registration Number based on the order in which they are detected. This order can be forced to occur in a given sequence by adding modules one at a time or it can be allowed to happen randomly. For further details, see the *Building a System*, *Maintaining a System*, and *Expanding a System* sections of this manual.

The system does not identify I/O modules by physical position on a backbone, only by registration sequence. MAQ20-940 ReDAQ Shape Software for MAQ20 provided by Dataforth shows a graphical representation of a system based on registration sequence and not by physical position. Tools within the software package allow the user to reassign Registration Numbers thereby making graphical representations match physical location for a single, local backbone.

Module Detect: A write to the Module Detect register at I/O module register address 98 plus the module offset based on Registration Number will blink the STAT LED on the top angled surface of the module at a 5Hz rate for 5 seconds so the module location in a system can be visually identified.

Each module is assigned an address space of 2000 addresses based on the Registration Number and starting at address 2000. I/O module with Registration Number 1 is assigned address space 2000 – 3999, I/O module with Registration Number 2 is assigned address space 4000 – 5999 and so on. The starting address for the module is very important because this is the offset address that must be added to the addresses listed in the I/O module register address map to know where data for that module is located within the system level address map. The MAQ20-COMx Communication Module is always assigned a Registration Number of 0 and cannot be re-sequenced.

**Table 4: MAQ20 System Register Address Range & Module Register Address Range**

| Registration Number | System Register Address Range | Module Register Address Range | Register Address Offset |
|---|---|---|---|
| 0 | 0 to 1999 | 0 to 1999 | 0 |
| 1 | 2000 to 3999 | 0 to 1999 | 2000 |
| 2 | 4000 to 5999 | 0 to 1999 | 4000 |
| 3 | 6000 to 7999 | 0 to 1999 | 6000 |
| … | … | … | … |
| 24 | 48000 to 49999 | 0 to 1999 | 24000 |

The automated registration process can be disabled, and I/O modules can be registered using a manual process if required by an application. Refer to the MAQ20 I/O Module Registration section of the *MA1040 MAQ20 Communications Module Hardware User Manual* for details.

The standard mode of operation is called Continuous Scan Mode. All channels are enabled, and input readings are taken by sending a read request command to the module. In Burst Scan Mode, channels can be selectively enabled.

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Channel Data is stored starting at module register address 1000, which is system register address 2000 * R + 1000, where R is the module Registration Number.

**Table 5: MAQ20-BRDG1 Address Map Excerpt – Module Data**

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1000 | R | 8 | Channel Data | Data for 4 Signal Channels. 24-bit data LSB at 100x, MSB at 100x+1. 16-bit data at 100x, 100x+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1008 | R | 8 | Excitation Data | Data for 4 Excitation Channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx, 10xx+2. | 0 to $2^{32-1}$ or 0 to $2^{16}$-1 | INT32 / INT16 |

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 6. Assume 24-bit data and read Signal Data and Excitation Data for Channel 0.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 6 = 12000

Read from system register address 12000+1000 = 13000 the Channel 0 Signal Data LSB
Read from system register address 12000+1001 = 13001 the Channel 0 Signal Data MSB

Read from system register address 12000+1008 = 13008 the Channel 0 Excitation Data LSB
Read from system register address 12000+1009 = 13009 the Channel 0 Excitation Data MSB

The MAQ20-940 ReDAQ Shape Software for MAQ20 has a utility which allows the user to reassign Registration Numbers to I/O Modules in a system. This can be used to rearrange the way I/O modules are displayed in the software if the Alternate Registration Processes have been used instead of the Standard Registration Processes. These are described in the *Building a System, Maintaining a System,* and *Expanding a System* sections of this manual.

ReDAQ Shape Software for MAQ20 presents a graphical representation of the system on the Acquire panel as shown in Figure 6. I/O modules are displayed sequentially left to right in the order they were registered. The display does not represent physical position and will not show physical vacant positions between I/O modules. The system graphic shows a 24-position backbone regardless of the backbone or combination of backbones used in a system.

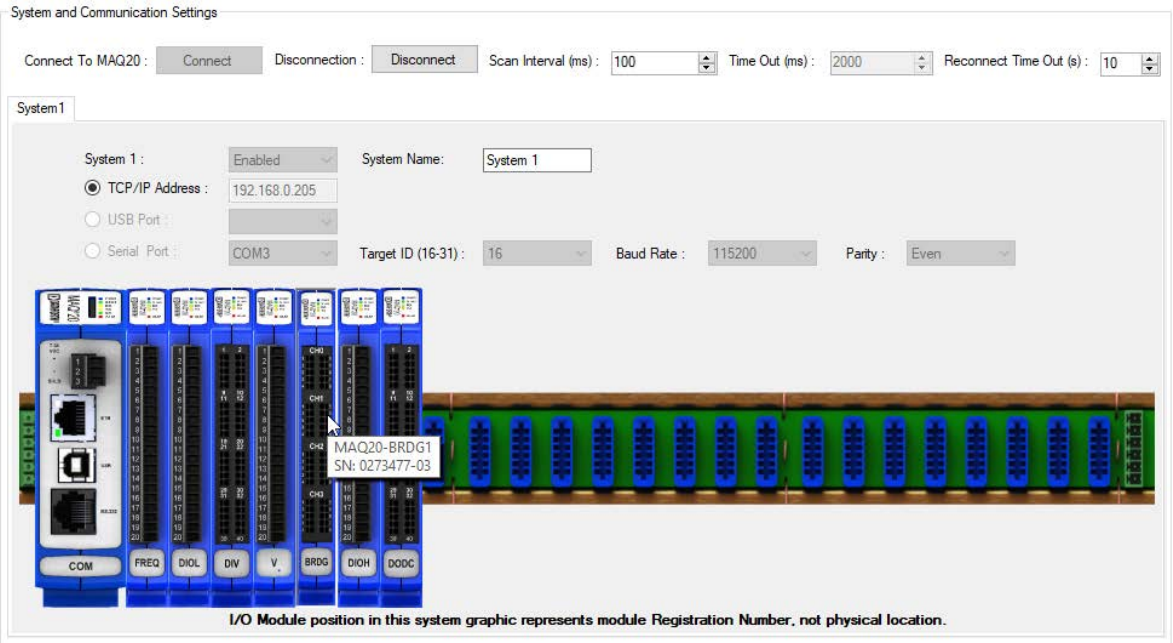
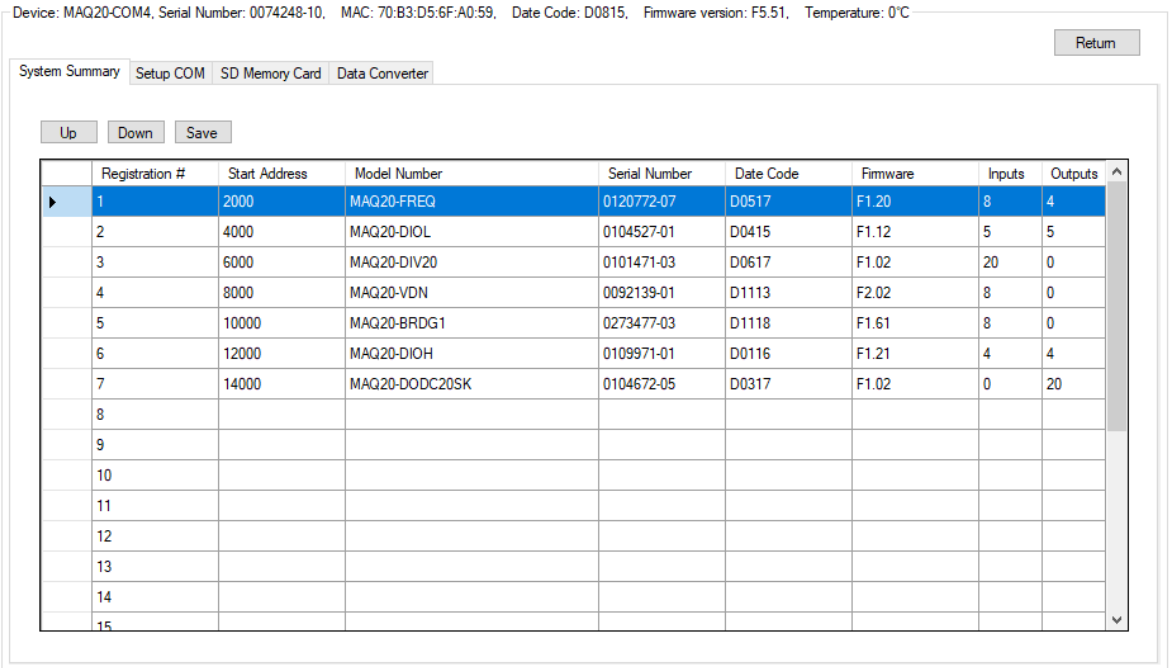



**Figure 6: MAQ20-940 ReDAQ Shape for MAQ20 Main Configuration Screen**

To view the registration sequence, click on the MAQ20-COMx graphic to obtain the system panel shown in Figure 7.




| | Registration # | Start Address | Model Number | Serial Number | Date Code | Firmware | Inputs | Outputs |
|---|---|---|---|---|---|---|---|---|
| ▶ | 1 | 2000 | MAQ20-FREQ | 0120772-07 | D0517 | F1.20 | 8 | 4 |
| | 2 | 4000 | MAQ20-DIOL | 0104527-01 | D0415 | F1.12 | 5 | 5 |
| | 3 | 6000 | MAQ20-DIV20 | 0101471-03 | D0617 | F1.02 | 20 | 0 |
| | 4 | 8000 | MAQ20-VDN | 0092139-01 | D1113 | F2.02 | 8 | 0 |
| | 5 | 10000 | MAQ20-BRDG1 | 0273477-03 | D1118 | F1.61 | 8 | 0 |
| | 6 | 12000 | MAQ20-DIOH | 0109971-01 | D0116 | F1.21 | 4 | 4 |
| | 7 | 14000 | MAQ20-DODC20SK | 0104672-05 | D0317 | F1.02 | 0 | 20 |
| | 8 | | | | | | | |
| | 9 | | | | | | | |
| | 10 | | | | | | | |
| | 11 | | | | | | | |
| | 12 | | | | | | | |
| | 13 | | | | | | | |
| | 14 | | | | | | | |
| | 15 | | | | | | | |

**Figure 7: Module Registration using MAQ20-940 ReDAQ Shape for MAQ20**

Registration Numbers listed in the left column refer to the position where the software has registered the I/O module. Registration Number will not necessarily be the same as the physical

position of the module in the system. To change the Registration Number of an I/O module, click the box in the left column next to the Registration Number, then use the Up and Down buttons to move the module within the sequence. The system automatically reassigns the I/O modules above and below the one moved. Repeat for other modules if desired. The MAQ20-COMx module always has Registration Number 0 and cannot be moved. Press 'Save' to save the new configuration. The new registration sequence is permanent across power cycles and any other system configuration as long as I/O modules are not removed from or added to a system.

## 13.0 Signal Gain and Conversion to Engineering Units

The MAQ20-BRDG1 module has a factory default input signal range of -100mV to +100mV. 24-bit data conversion provides a high level of accuracy and resolution over this signal range. The input signal range can be set independently for each channel to ±100mV, ±50mV, ±25mV, ±12.5mV or ±8.33mV. Over-range and Under-range up to 2% beyond the specified input values will be measured. Input signal range is set on a channel-by-channel basis by writing the appropriate code to a module register. The Range Table following the Address Map at the end of this manual shows the signal ranges and the signal to counts mapping. An excerpt from the Range Table is shown below.

**Table 6: Excerpt from Range Table**

**Sampling Rate = 1kS/s, 2kS/s, 4kS/s, 8kS/s, 16kS/s**

| Signal Gain Code | Signal Gain | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|
| 0 (Default) | 1 | -100mV to +100mV | -8197767 to 8197767 | -102.328mV to +102.328mV | -8388608 to 8388607 |
| 1 | 2 | -50mV to +50mV | -8197767 to 8197767 | -51.164mV to +51.164mV | -8388608 to 8388607 |
| 2 | 4 | -25mV to +25mV | -8197767 to 8197767 | -25.582mV to +25.582mV | -8388608 to 8388607 |
| 3 | 8 | -12.5mV to +12.5mV | -8197767 to 8197767 | -12.791mV to +12.791mV | -8388608 to 8388607 |
| 4 | 12 | -8.33mV to +8.33mV | -8197767 to 8197767 | -8.527mV to +8.527mV | -8388608 to 8388607 |

**Sampling Rate = 32kS/s**

| Signal Gain Code | Signal Gain | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|
| 0 (Default) | 1 | -100mV to +100mV | -32023 to 32023 | -102.328mV to +102.328mV | -32768 to 32767 |
| 1 | 2 | -50mV to +50mV | -32023 to 32023 | -51.164mV to +51.164mV | -32768 to 32767 |
| 2 | 4 | -25mV to +25mV | -32023 to 32023 | -25.582mV to +25.582mV | -32768 to 32767 |
| 3 | 8 | -12.5mV to +12.5mV | -32023 to 32023 | -12.791mV to +12.791mV | -32768 to 32767 |
| 4 | 12 | -8.33mV to +8.33mV | -32023 to 32023 | -8.527mV to +8.527mV | -32768 to 32767 |

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Input Range is stored starting at module register address 100, which is system register address 2000 * R + 100, where R is the module Registration Number. Channel Data is stored starting at module register address 1000, which is system register address 2000 * R + 1000. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 100 | R/W | 4 | Input Range | 0 = ±100mV (Default)<br>1 = ±50mV<br>2 = ±25mV<br>3 = ±12.5mV<br>4 = ±8.33mV | 0 to 4 | INT16 |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, $V_{exc}$, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1000 | R | 8 | Channel Data | Data for 4 Signal Channels. 24-bit data LSB at 100x, MSB at 100x+1. 16-bit data at 100x, 100x+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |

To change the input range for each of the four input channels, write 0 to 4 to the module registers at Address 100 to 103. Note that this address block is offset by 2000 * R. Once an input range selection is made it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Set channel 0 for an input range of ±100mV, channel 1 for an input range of ±25mV and channels 2 and 3 for an input range of ±12.5mV. Obtain the current reading in counts for channel 0 input signal and convert to Engineering units.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

1.) Write to system register address 4000+100 = 4100 a data value of 0 to set Ch 0 input range = ±100mV

2.) Write to system register address 4000+101 = 4101 a data value of 2 to set Ch 1 input range = ±25mV

3.) Write to system register address 4000+102 = 4102 a data value of 3 to set Ch 2 input range = ±12.5mV

4.) Write to system register address 4000+103 = 4103 a data value of 3 to set Ch 3 input range = ±12.5mV

When signal sample rates of 1kS/s, 2kS/s, 4kS/s, 8kS/s and 16kS/s are used, sampled data will be 24 bits. LSB data is stored at the lower address and MSB data is stored at the higher address.

Assume the data is 24-bit.

1.) Read from system register address 4000 + 1000 = 5000 the Channel 0 Signal Data LSB

2.) Read from system register address 4000 + 1001 = 5001 the Channel 0 Signal Data MSB

If the data read from Channel 0 Signal Data LSB is 23154 counts and the data read from Channel 0 Signal Data MSB is 106 counts, the input signal is:

| | |
|---|---|
| Ch 0 LSB convert to binary | 0101101001110010 |
| Ch 0 MSB convert to binary | 0000000001101010 |
| Ch 0 24-bit representation | MSB + LSB = 011010100101101001110010 |
| Ch 0 Decimal equivalent | 6969970 |

6969970 counts * (+100mV - -100mV)/(8197767 counts - -8197767 counts) = 85.023mV

When the signal sample rate of 32kS/s is used, sampled data will be 16 bits.

Assume a sample rate of 32kS/s is used and obtain 16-bit data.

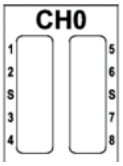
Read from system register address 4000+1000 = 5000 the Channel 0 Signal Data

If the data read from Channel 0 is 23154 counts, the input signal is:

23154 counts * (+100mV - -100mV)/(32023 counts - -32023 counts) = 72.304mV

## 14.0 Sensor Excitation

A single source is provided for excitation of one to four strain gages. Internal to the module, the +EXC and –EXC source connections for each channel are common. Each of the four channels has a dedicated excitation sense connection which measures the excitation voltage at the field terminal blocks. See the *Remote Sense* section of this manual for sensor excitation remote sense. The excitation voltage source can be set to 2.5V, 3.3V, 5.0V or 10.0V. The value selected will be the same for all four channels. The excitation is provided on Terminals 1 and 2 for each of the four channels. Sensor Excitation is set by writing the appropriate code to a module register.




| | FIELD CONNECTION | TERMINAL | TERMINAL | FIELD CONNECTION |
|---|---|---|---|---|
| CHANNEL 0 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |

**Figure 8: Field Terminal Block Connections**

Each channel has continuous excitation overload protection up to 30Vrms as well as transient overload protection to prevent module or system damage in cases of inadvertent wiring errors, ESD, or other external faults. Basic circuit topology and full bridge sensor connection are shown in Figure 9 below.

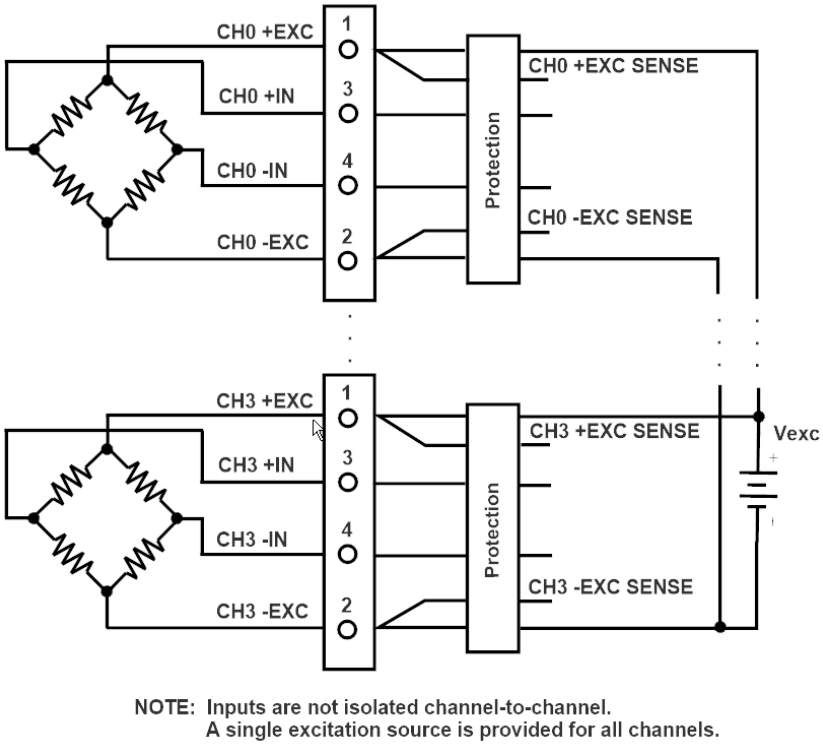



**Figure 9: Excitation Circuit Topology**

The total load that can be delivered by the source is 80mA for normal operating conditions. If the ambient temperature of the module is +80°C or higher, the total load is de-rated to 60mA. Bridge resistance is specified as 100Ω to 1kΩ. Assuming identical sensors are used on each channel, the minimum bridge element resistance can be expressed using this formula with results shown in Table 7.

Full Bridge Sensor, Tambient = +25°C to +80°C
Rbridge element (min) = Vexc / 80mA * Number of Sensors

Full Bridge Sensor, Tambient = +80°C to +85°C
Rbridge element (min) = Vexc / 60mA * Number of Sensors

Half or Quarter Bridge Sensor, Tambient = +25°C to +80°C
Rbridge element (min) = Vexc / 80mA * Number of Sensors / 2

Half or Quarter Bridge Sensor, Tambient = +80°C to +85°C
Rbridge element (min) = Vexc / 60mA * Number of Sensors / 2

**Table 7: Minimum Bridge Resistance, Full Bridge Sensor, Tambient = +25°C to +80°C**

| Vexc | Min Bridge Element Resistance vs. Number of Full Bridge Sensors | | | | Min Bridge Element Resistance vs. Number of Half or Quarter Bridge Sensors | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |
| 2.5V | 100Ω | 100Ω | 100Ω | 125Ω | 100Ω | 100Ω | 100Ω | 100Ω |
| 3.333V | 100Ω | 100Ω | 125Ω | 167Ω | 100Ω | 100Ω | 100Ω | 100Ω |
| 5.0V | 100Ω | 125Ω | 188Ω | 250Ω | 100Ω | 100Ω | 100Ω | 125Ω |
| 10.0V | 125Ω | 250Ω | 375Ω | 500Ω | 100Ω | 125Ω | 188Ω | 250Ω |

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Excitation Voltage setting is stored starting at module register address 600, which is system register address 2000 * R + 600, where R is the module Registration Number. Excitation Voltage readings are stored starting at module register address 1008, which is system register address 2000 * R + 1008. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| **Address Range 100 - 699: Module Configuration** | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, Vexc, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 600 | R/W | 1 | Excitation Voltage | 0 = 2.5V, 1 = 3.3V, 2 = 5V, 3 = 10V. Default = 0. | 0 to 3 | INT16 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1008 | R | 8 | Excitation Data | Data for 4 Excitation Channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx, 10xx+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |

To change the sensor excitation voltage, write 0 to 3 to Address 600. Note that this address is offset by 2000 * R. Once an excitation selection is made it can be saved to local memory by writing a 0 to module register 119.

Excitation voltage measurements are stored starting at module register address 1008.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Set the sensor excitation voltage for all channels to 3.3V. Obtain the current reading in counts for channel 0 excitation voltage and convert to Engineering units.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

Write to system register address 4000+600 = 4600 a data value of 2 to set Vexc = 3.3V

When signal sample rates of 1kS/s, 2kS/s, 4kS/s, 8kS/s and 16kS/s are used, sampled data will be 24 bits. LSB data is stored at the lower address and MSB data is stored at the higher address.

Assume the default sample rate of 4kS/s is used and obtain 24-bit data.

Read from system register address 4000 + 1008 = 5008 the Channel 0 Excitation Data LSB
Read from system register address 4000 + 1009 = 5009 the Channel 0 Excitation Data MSB

If the data read from Channel 0 Excitation Data LSB is 43516 counts and the data read from Channel 0 Excitation Data MSB is 26 counts, the excitation signal is:

| | |
|---|---|
| Ch 0 LSB convert to binary | 1010100111111100 |
| Ch 0 MSB convert to binary | 0000000000011010 |
| Ch 0 24-bit representation | MSB + LSB = 000110101010100111111100 |
| Ch 0 Decimal equivalent | 1747452 |

Vexc = 1747452 / 8388608 * 16 = 3.3V

When the signal sample rate of 32kS/s is used, sampled data will be 16 bits.

Assume a sample rate of 32kS/s is used and obtain 16-bit data.

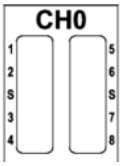
Read from system register address 4000+1008 = 5008 the Channel 0 Excitation Data

If the data read from Channel 0 Excitation Data is 6826 counts, the excitation signal is:

Vexc = 6826 / 32768 * 16 = 3.3V

## 15.0 Full Bridge, Half Bridge & Quarter Bridge Sensors

The MAQ20-BRDG1 module interfaces to full bridge sensors using the +EXC, -EXC, +IN and –IN terminals. The module has internal bridge completion circuits on each of the four input channels for interfacing to half bridge and quarter bridge sensors using the +EXC, -EXC and +IN terminals. Half bridge and quarter bridge completion is enabled on a channel-by-channel basis by writing to a module register.

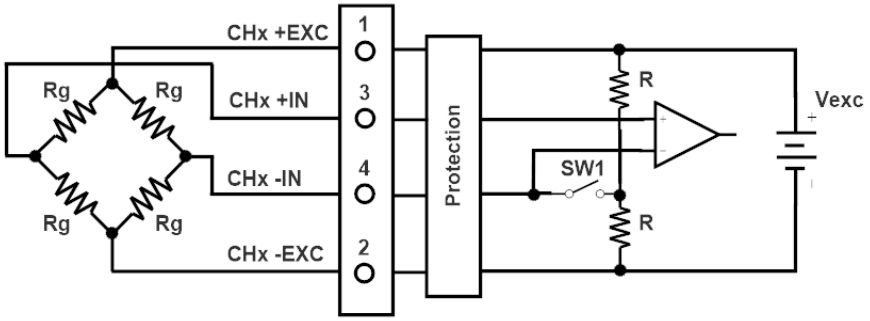



| | FIELD CONNECTION | TERMINAL | TERMINAL | FIELD CONNECTION |
|---|---|---|---|---|
| CHANNEL 0 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |

**Figure 9: Field Terminal Block Connections**

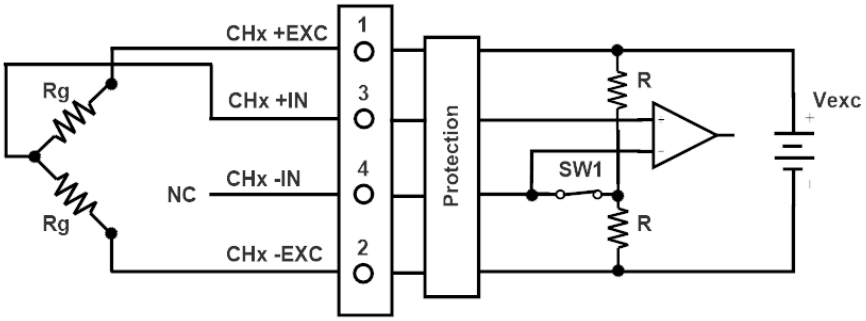
Each channel has continuous signal and excitation overload protection for up to 30Vrms as well as transient overload protection to prevent module or system damage in cases of inadvertent wiring errors, ESD, or other external faults.

A single source is provided for excitation of one to four strain gages. Internal to the module, the +EXC and –EXC source connections for each channel are common. A single set of bridge completion resistors is provided for connection to one to four strain gages. If bridge completion is enabled on more than one channel, the –IN terminals for all channels with bridge completion enabled will be connected together. This may affect signal integrity in some applications. The resistance of the internal bridge completion resistors, R, is 4.9kΩ. Basic circuit topology and sensor connection is shown in Figure 10, Figure 11 and Figure 12.



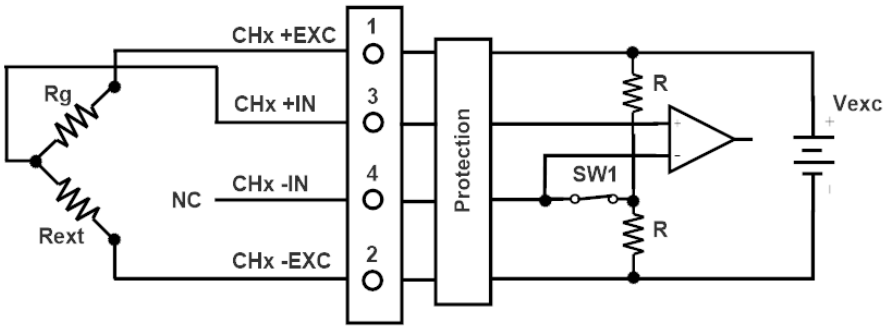

NOTES: Rg represents active strain elements.
SW1 is open for connection to Full Bridge sensors.

**Figure 10: Full Bridge Sensor Connection**




NOTES: Rg represents active strain elements.
SW1 is closed for connection to Half Bridge sensors.

**Figure 11: Half Bridge Sensor Connection**




NOTES: Rg represents the single active strain element.
SW1 is closed for connection to Quarter Bridge sensors.
Rext is a customer supplied external resistor.
The resistance of Rext must be equal to Rg.
Rext can be located at the input terminal block or remote with Rg.

**Figure 12: Quarter Bridge Sensor Connection**

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Bridge Configuration is stored starting at module register address 610, which is system register address 2000 * R + 610, where R is the module Registration Number. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, Vexc, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 610 | R/W | 4 | Bridge Configuration | 0 = Half Bridge, 1 = Full Bridge. Default = 1. | 0 or 1 | INT16 |

To enable or disable the internal bridge completion resistors for each of the four input channels, write a 0 or 1 to the module registers at Address 610 to 613. Note that this address block is offset by 2000 * R. Once a half bridge completion selection is made it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Assume full bridge sensors are used on Channels 0 and 1, a half bridge sensor is used on Channel 2, and a quarter bridge sensor is used on Channel 3. Enable the Half Bridge completion resistors on Channels 2 and 3 for correct interface to the sensors.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

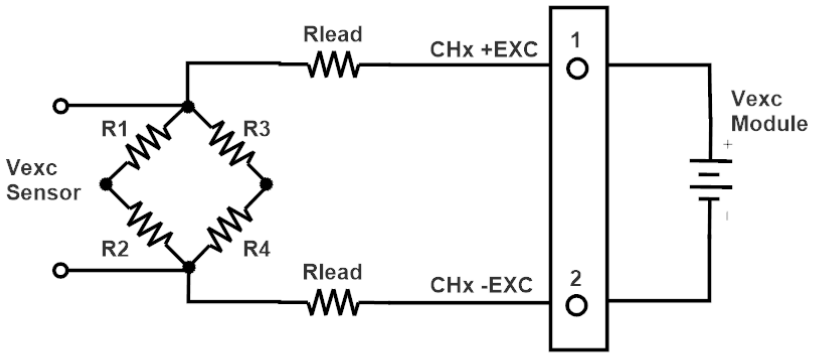
1.) Write to system register address 4000+612 = 4612 a value of 0 to enable bridge completion on Ch 2

2.) Write to system register address 4000+613 = 4613 a value of 0 to enable bridge completion on Ch 3

## 16.0 Remote Sense

Common excitation voltages for strain gages are 2.5V to 10V. Most strain gage signal conditioners use a four-wire connection to the bridge to simplify field wiring. Four wire connections require the excitation voltage source to be accurate and stable over temperature, time, and load. They also require short connections between the strain gage and signal conditioner to reduce errors caused by voltage drops across wiring resistance. The MAQ20-BRDG1 module has the ability to use remote sensing to eliminate the requirement for a precision excitation source and concerns over leadwire resistance.

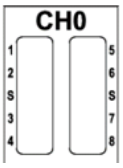
Standard connection between the MAQ20-BRDG1 module and a strain gage is made using a four-wire connection as shown in the *Sensor Excitation* section of this manual. This connection is recommended for most applications. When high precision is required or leadwire resistance is a concern, remote sense using six wire connection will eliminate errors. Another method used to eliminate errors is outlined in the *V/V Ratiometric Signal Representation* section of this manual. To use the Remote Sense feature, simply connect field terminals 5 and 6 to the strain gage remotely at the location where the strain gage is installed.




NOTE: For remote located sensors, Vexc at the sensor is not equal to Vexc at the field terminal blocks due to leadwire resistance error.

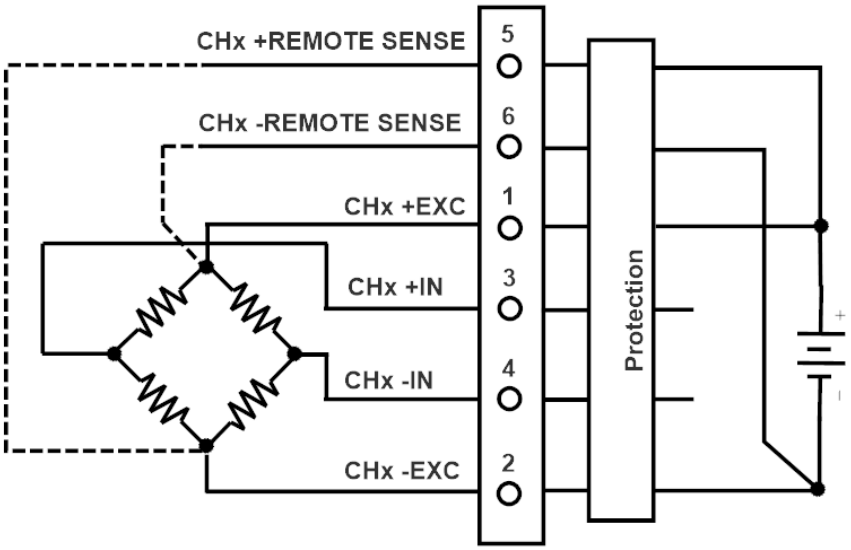
**Figure 13: Remote Sensor Error Sources**

A single source is provided for excitation of one to four strain gages. Internal to the module, the +EXC and –EXC source connections for each channel are common. Each of the four channels has a dedicated excitation remote sense connection for measurement of the excitation voltage at the remote located sensor.




| | FIELD CONNECTION | TERMINAL | TERMINAL | FIELD CONNECTION |
|---|---|---|---|---|
| CHANNEL 0 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |

**Figure 14: Field Terminal Block Connections**




NOTES: When Remote Sense terminals are connected, module operates in 6-wire mode.
When Remote Sense terminals are not used, module operates in 4-wire mode.
No module configuration is required for these two modes.

**Figure 15: MAQ20-BRDG1 Remote Sense Connection**

## 17.0 Shunt Calibration

When strain gages are used to measure stress and strain, calibration is required to attain the highest levels of accuracy and linearity. Typical sources of error that require compensation are leadwire resistance and variance between sensors. Once a strain gage is fixed in place to measure a given stress or strain, it can be difficult to force the bridge into the full scale positive or negative conditions for the purposes of calibration or verification by applying precision mechanical input. A commonly used alternative is to force a known imbalance in the strain gage using fixed resistors, creating a precise and predictable strain gage output. This indirect method of calibration is called Shunt Calibration.

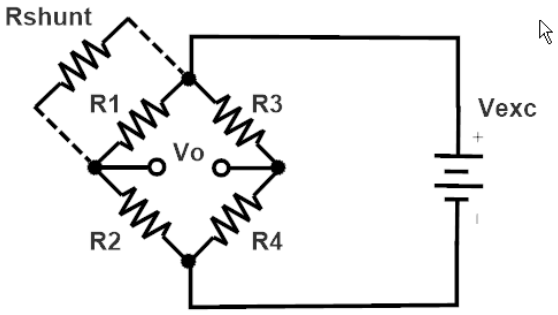
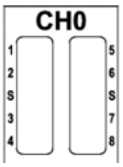


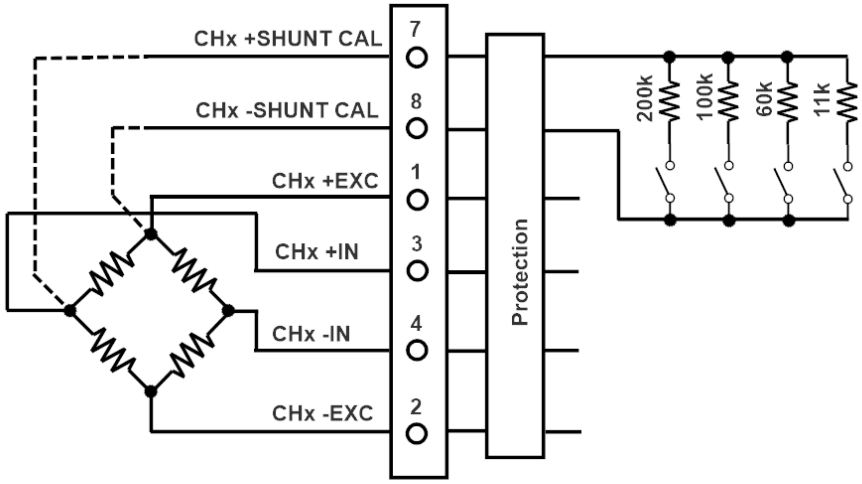

**Figure 16: Shunt Calibration**

Each input channel on the MAQ20-BRDG1 module has three internal resistors accessible through Terminals 7 and 8 for use in shunt calibration. Each channel also has the option to use an external resistor for shunt calibration. These four options are set by writing the appropriate code to a module register.




| | FIELD CONNECTION | TERMINAL | TERMINAL | FIELD CONNECTION |
|---|---|---|---|---|
| CHANNEL 0 | +EXC | 1 | 5 | +REMOTE SENSE |
| | -EXC | 2 | 6 | -REMOTE SENSE |
| | SHIELD | S | S | SHIELD |
| | +IN | 3 | 7 | +SHUNT CAL |
| | -IN | 4 | 8 | -SHUNT CAL |

**Figure 17: Field Terminal Block Connections**




NOTES: Four shunt calibration resistors are provided for each channel, CH0 - CH3.
Resistor banks are separate and isolated for each channel.
For external shunt resistor, place the resistor in series with terminal 7 or terminal 8 and use internal 11k ohm resistor.

**Figure 18: MAQ20-BRDG1 Internal Shunt Calibration Resistors**

Formulas for use of shunt calibration resistors to simulate microstrain are:
When the bridge is balanced, (Vout/Vin)unstrained = 0

Vr = [(Vout/Vin)strained - (Vout/Vin)unstrained]

Full Bridge Ɛ = -Vr/GF
Half Bridge Ɛ = -2Vr/GF
Quarter Bridge Ɛ = -4Vr/(GF(1+2Vr))

GF = Gage Factor. Common value used is 2.
Rg = Gage element nominal resistance. Typical values are 120 ohm, 350 ohm, 1000 ohm.
Shunt calibration resistor value for simulated microstrain, Ɛ

$Rc = Rg*10^6/GF*Ɛ - Rg$

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Shunt Calibration Resistor selection is stored starting at module register address 620, which is system register address 2000 * R + 620, where R is the module Registration Number. Shunt Calibration enable is stored at module register address 624, which is system register address 2000 * R + 624. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, Vexc, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 620 | R/W | 4 | Shunt Calibration Resistors | 0 = 60kohm, 1 = 100kohm, 2 = 200kohm and 3 = External. Default = 0. | 0 to 3 | INT16 |
| 624 | R/W | 1 | Shunt Calibration On/Off | 0 = On, 1 = Off Default = 1 | 0 or 1 | INT16 |

To set an internal shunt calibration resistor for each of the four input channels, write 0 to 3 to the module registers at Address 620 to 623. Note that this address block is offset by 2000 * R. To enable or disable all internal shunt calibration resistors for each of the four input channels, write a 0 or 1 to Address 624. Note that this address is offset by 2000 * R. Once a shunt calibration resistor and On/Off state selection is made, it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Assume input terminals 7 and 8 have been connected to one of the sensor gage elements. Set shunt calibration resistance of 60kohm on Channel 0 and 200kohm on Channel 3. Enable the shunt calibration function to provide simulated bridge strain.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

1.) Write to system register address 4000+620 = 4620 a data value of 0 to set 60kohm shunt cal on Ch 0
2.) Write to system register address 4000+623 = 4623 a data value of 2 to set 200kohm shunt cal on Ch 3
3.) Write to system register address 4000+624 = 4624 a data value of 0 to enable shunt calibration function

## 18.0 Auto Zero

When strain gages are used to measure stress and strain, calibration is required to attain the highest levels of accuracy and linearity. One typical source of error that requires compensation is bridge imbalance. Once a strain gage is fixed in place to measure a given stress or strain, variations in nominal resistance of bridge elements and leadwire resistance for remote located bridge elements will result in a non-zero bridge output when no stress or strain is applied. Another common situation is the need to measure a stress or strain from a given reference state, such as the tare function on a weigh scale.

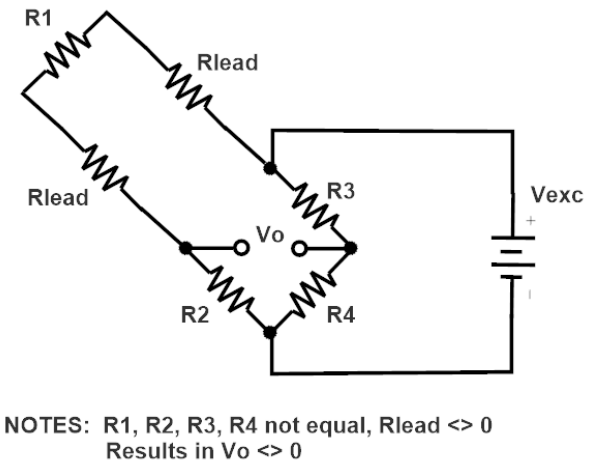



**Figure 19: Bridge Imbalance**

The MAQ20-BRDG1 module simplifies compensation for this error source by providing independent Auto Zero on each of the four input channels. With the bridge in a reference state, enabling the Auto Zero function will null out bridge imbalance and the module will report a reading of zero. Disabling the Auto Zero function will result in the module reporting the true bridge imbalance reading.

The MAQ20-BRDG1 Address Map is found at the end of this manual. An excerpt from the Address Map is shown below. Auto Zero Enable is stored starting at module register address 626, which is system register address 2000 * R + 626, where R is the module Registration Number. Readings prior to auto zero enable are stored starting at module register address 630, which is system register address 2000 * R + 630. Refer to the MAQ20 I/O Module Registration section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 626 | R/W | 1 | Auto Zero Ch 0 Enable | 1 = Set new zero value<br>0 = Clear zero<br>Default = 0 | 0 or 1 | INT16 |
| 627 | R/W | 1 | Auto Zero Ch 1 Enable | 1 = Set new zero value<br>0 = Clear zero<br>Default = 0 | 0 or 1 | INT16 |
| 628 | R/W | 1 | Auto Zero Ch 2 Enable | 1 = Set new zero value<br>0 = Clear zero<br>Default = 0 | 0 or 1 | INT16 |
| 629 | R/W | 1 | Auto Zero Ch 3 Enable | 1 = Set new zero value<br>0 = Clear zero<br>Default = 0 | 0 or 1 | INT16 |
| 630 | R/W | 8 | Auto Zero Values | 4 channel Auto Zero values. 24-bit data LSB at 63x, MSB at 63x+1. 16-bit data at 63x. | | INT32 / INT16 |

To enable auto zero for each of the four input channels, write a 1 to the module registers at Address 626 to 629. Note that this address block is offset by 2000 * R. When auto zero is enabled, the current readings at module registers 1000 to 1008 for the channel selected are stored at module registers 630 to 637 and new readings stored at module registers 1000 to 1008 are compensated using the stored auto zero reading. Once an auto zero selection is made it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Assume bridge imbalance results in a 24-bit reading of 25000 counts on Channel 0 and 50000 counts on Channel 3. Enable the auto zero function on Channel 0 and Channel 3 to provide compensation for bridge imbalance.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

Write to system register address 4000+626 = 4626 a data value of 1 to enable auto zero on Ch 0

The previous value of 25000 counts at system registers 4000+1000 = 5000 and 4000+1001 = 5001 will be stored at system registers 4000+630 = 4630 and 4000+631 = 4631.

New readings at system registers 5000 and 5001 will be zero counts. Any change in bridge output from 25000 counts will show at system registers 5000 and 5001 as a change from zero counts.

Write to system register address 4000+629 = 4629 a data value of 1 to enable auto zero on Ch 3

The previous value of 50000 counts at system registers 4000+1006 = 5006 and 4000+1007 = 5007 will be stored at system registers 4000+636 = 4636 and 4000+637 = 4637.

New readings at system registers 5006 and 5007 will be zero counts. Any change in bridge output from 50000 counts will show at system registers 5006 and 5007 as a change from zero counts.

Write to system register address 4000+626 = 4626 a data value of 0 to disable auto zero on Ch 0

Values at system registers 4630 and 4631 will be zero counts and new readings at system registers 5000 and 5001 will be 25000 counts.

## 19.0 Signal Sample Rate

The MAQ20-BRDG1 module uses eight analog-to-digital converters (ADC) to measure signal and excitation for the four input channels. The ADCs have configurable sample rate for storage of data internal to the module. All ADCs are set to the same sample rate. Sampled data is normally retrieved from the module as described in the *Continuous Scan Mode* section of this manual. In Continuous Scan Mode, channel scan rate is limited by the system backbone communications rate and the number of MAQ20 I/O modules in a system. When faster data capture rates are required, the MAQ20-BRDG1 module offers another mode described in the *Burst Scan Mode* section of this manual. Burst Scan stores short periods of high-speed data capture in module volatile memory, then data is downloaded to a host PC.

Sample rate ranges from 1kS/s to 32kS/s. When signal sample rates of 1kS/s, 2kS/s, 4kS/s, 8kS/s and 16kS/s are used, sampled data will be 24 bits with LSB data stored at the lower address and MSB data is stored at the higher address. When the signal sample rates of 32kS/s is used, sampled data will be 16 bits.

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Sampling Rate and Resolution setting is stored at module register address 678, which is system register address 2000 * R + 678, where R is the module Registration Number. Channel Data is stored starting at module register address 1000, which is system register address 2000 * R + 1000. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, Vexc, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 678 | R/W | 1 | Sampling Rate & Resolution | 0 = future use<br>1 = 16bit, 32kS/s<br>2 = 24bit, 16kS/s<br>3 = 24bit, 8kS/s<br>4 = 24bit, 4kS/s (Default)<br>5 = 24bit, 2kS/s<br>6 = 24bit, 1kS/s | 1 to 6 | INT16 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1000 | R | 8 | Channel Data | Data for 4 Signal Channels. 24-bit data LSB at 100x, MSB at 100x+1. 16-bit data at 100x, 100x+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |

To set the module internal sampling rate and data conversion resolution, write 1 to 6 to module register address 678. Note that this address is offset by 2000 * R. Once an internal sample rate selection is made it can be saved to local memory by writing a 0 to module register 119.

*Example:* A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. The input signal range is ±100mV. Set the internal sampling rate to 1kS/s and convert the measured Ch 0 input signal counts to engineering units.

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

Write to system register address 4000 + 678 = 4678 a data value of 6 to set 1kS/s sampling rate and 24-bit data conversion

Read from system register address 4000+1000 = 5000 the Channel 0 Signal Data LSB
Read from system register address 4000+1001 = 5001 the Channel 0 Signal Data MSB

If the data read from Channel 0 Signal Data LSB is 23154 counts and the data read from Channel 0 Signal Data MSB is 106 counts, the input signal is:

| | |
|---|---|
| Ch 0 LSB convert to binary | 0101101001110010 |
| Ch 0 MSB convert to binary | 0000000001101010 |
| Ch 0 24-bit representation | MSB + LSB = 011010100101101001110010 |
| Ch 0 Decimal equivalent | 6969970 |

6969970 counts * (+100mV - -100mV)/(8197767 counts - -8197767 counts) = 85.023mV

*Example:* A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. The input signal range is ±100mV. Set the internal sampling rate to 32kS/s and convert the measured Ch 0 input signal counts to engineering units.

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

Write to system register address 4000+678 = 4678 a data value of 1 to set 32kS/s sampling rate and 16-bit data conversion

Read from system register address 4000+1000 = 5000 the Channel 0 Signal Data

If the data read from Channel 0 is 23154 counts, the input signal is:

23154 counts * (+100mV - -100mV)/(32023 counts - -32023 counts) = 72.304mV

## 20.0 Continuous Scan Mode

MAQ20-BRDG1 modules have eight analog-to-digital converters which continuously scan the four input channels and excitation voltage source and store the data in local memory. As new data is acquired, previous sampled data is continuously overwritten such that local memory always has the most recent data. The sample rate is 4kS/s default and is user configurable from 1kS/s to 32kS/s as described in the *Signal Sample Rate* section of this manual. When a channel data read command is received, data for all channels is retrieved from local memory and returned in a single response. A standard command-response cycle to acquire analog or digital data from all channels of a single input module takes 6ms. Channel scan rate at the system level depends on the number of MAQ20 I/O modules installed in a system. As more modules are added to a system, the scan rate for an individual channel decreases.

The following calculation is used to determine channel scan rate for each of the four input channels.

Module Scan Rate = Scans / s = Number of MAQ20 I/O modules in a system / 6ms

Each command/response cycle, four channels of data are acquired. Net scan rate is then expressed as:

Net Scan Rate = Scans / s * Number of channels

*Example: Determine the MAQ20-BRDG1 per channel scan rate for the following system:*
*MAQ20-COM4*
*MAQ20-BRDG1*

Scan rate for each of the input channels is:

Scan Rate, Ch0 – Ch4 = 1 / 6ms = 167 Scans / s = 167 Hz

Each command/response cycle, four channels of data are acquired. Net scan rate is then expressed as:

Net Scan Rate = 167 Hz * 4 channels = 668 Ch / s

*Example: Determine the MAQ20-BRDG1 per channel scan rate for the following system:*
*MAQ20-COM4*
*MAQ20-BRDG1 #1 (4 channels)*
*MAQ20-BRDG1 #2 (4 channels)*
*MAQ20-VDN (8 channels)*
*MAQ20-BRDG1 #3 (4 channels)*

Scan rate for each of the input channels is:

Scan Rate, Ch0 – Ch4 = 1 / (6ms * 4 modules) = 42 Scans / s = 42 Hz

Each command/response cycle, four channels of data are acquired. Net scan rate is then expressed as:

Net Scan Rate, MAQ20-BRDG1 #1 = 42 Hz * 4 channels = 168 Ch / s
Net Scan Rate, entire system = 42 Hz * 20 channels = 840 Ch / s

## 21.0 Burst Scan Mode

MAQ20-BRDG1 modules have eight analog-to-digital converters which continuously scan the four input channels and excitation voltage source and store the data in local memory. The sample rate is 4kS/s default and is user configurable from 1kS/s to 32kS/s as described in the *Signal Sample Rate* section of this manual. Burst Scan Mode allows storage of all samples acquired over a short time period in internal volatile memory. Stored data is then transferred to the host computer in a separate operation. Upon power cycle or reset, all stored burst scan data is erased.

Burst Scan Mode user settable parameters are Channel Enable, Number of Samples to Read at the configured sample rate, FIR Filter Enable, and V/V Calculation Enable. Available Storage, Read Counter, and Read Data Buffer are used for status and data transfer operations.

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Burst Scan Mode settings are stored starting at module register address 1096, which is system register address 2000 * R + 1096, where R is the module Registration Number. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1096 | R/W | 1 | FIR filter Enable | Burst Scan Mode only<br>1 = Enabled 0 = Disabled<br>Default = 0 | 0 or 1 | INT16 |
| 1097 | R/W | 1 | V/V Calculation Enable | Burst Scan Mode only<br>1 = Enabled 0 = Disabled<br>Default = 0 | 0 or 1 | INT16 |
| 1098 | R/W | 2 | Number of Samples to Read | Burst Scan Mode Only 24-bit data, 2M sample max. 16-bit data, 4M sample max. LSB at 1098, MSB at 1099.<br>Default = 1000000 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1100 | R/W | 1 | Scan Start | Burst Scan Mode Only<br>1 = Start, 0 = Stop<br>Default = 0 | 0 or 1 | INT16 |
| 1101 | R/W | 4 | Channel Enable | Burst Scan Mode Only<br>Channels to be included in Burst Scan<br>1 = Enable, 0 = Disable<br>Default = 0 | 0 or 1 | INT16 |
| 1105 | R | 2 | Available Storage | Burst Scan Mode Only<br>Storage space remaining, expressed in number of samples. 24-bit data, 2M sample max. 16-bit data 4M sample max. LSB at 1105, MSB at 1106.<br>Default = 2000000 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1107 | R/W | 2 | Read Counter | Burst Scan Mode Only<br>Sample read counter. 24-bit data, 2M sample max. 16-bit data 4M sample max. LSB at 1107, MSB at 1108.<br>Default = 0 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1110 | R | 100 | Read Data Buffer | Burst Scan Mode Only<br>Used for data transfer from internal memory.<br>INT32: 24-bit data LSB at 1xxx, MSB at 1xxx+1.<br>INT16:16-bit data at 1xxx.<br>Float32: Integer part at 1xxx, fractional part at 1xxx+1. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 or -0.10 to +0.10 | INT32 / INT16 / Float32 |

To configure and run burst scan mode, write to module register addresses 1098 to 1101. Note that these addresses are offset by 2000 * R. Once burst scan settings are made, they can be saved to local memory by writing a 0 to module register 119.

*Example:* A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 2. Assume the internal sampling rate is 1kS/s. Configure and run a burst scan of 10,000 samples (10 seconds) on Channel 0 and Channel 1. Retrieve the data from module memory.

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 2 = 4000

Write to system register address 4000+1098 = 5098 a data value of 10000 to set the scan size
Write to system register address 4000+1100 = 5100 a data value of 1 to start the burst scan

Wait 10 seconds for the burst scan to complete.

Write to system register address 4000+1107 = 5107 a data value of 0 to initialize the data read counter

Read from system register address block 4000+1110 to 4000+1210 = 5110 to 5210 the first 100 samples

Read from system register address 4000+1107 = 5107 a data value of 100 which indicates read success

Save the samples to a file.

Repeat the block read from 5110 to 5210 a total of 100 times to retrieve the 10000 samples. After each block read, append the samples to the saved file.

The consolidated saved data can then be reviewed, plotted, analyzed, and used for any purpose.

The captured data will remain in the MAQ20-BRDG1 module memory and can be retrieved again using the steps above. Data is volatile and will be erased upon module power cycle or reset command.

To capture a new set of data, write a 1 to module register 1100.

To post process the data using the FIR filter function, write a 1 to register 1096.

To post process the data using the V/V Calculation function, write a 1 to register 1097. When V/V Calculation is enabled, data retrieved will be in Float32 format with integer part at register 1xxx and fractional part at register 1xxx+1.

## 22.0 Signal Average, Minimum & Maximum

The MAQ20-BRDG1 input circuitry is designed for low noise amplification of sensor signals. In some applications, sensor wiring and other environmental factors may induce noise on signal lines, or certain signal characteristics may want to be rejected. Applications may also require recording of minimum and maximum signal deviation for characterization or reporting purposes. For these reasons, user configurable signal averaging within the module is provided and minimum and maximum signal values are stored.

Signal averaging is set on a per-channel basis using the Average Weight coefficient. Average Weight is calculated as $2^x$ where x = 0 to 15 and the default value is x = 0. The running average is then calculated as follows:

$$\text{Average} = \text{Average} + \frac{\text{Sampled Value} - \text{Average}}{\text{Average Weight}}$$

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Signal Average Weight is stored starting at module register address 120, which is system register address 2000 * R + 120, where R is the module Registration Number. Signal Minimum, Maximum, and Average readings are stored starting at module register address 1030, which is system register address 2000 * R + 1030. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, Vexc, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 120 | R/W | 8 | Average Weight | Weight for Average Calculation. Default = 0. | 0 to 15 | INT16 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1030 | R/W | 8 | Signal Data Minimum | Minimum value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = -f.s. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1050 | R/W | 8 | Signal Data Maximum | Maximum value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = +f.s. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1070 | R/W | 8 | Signal Data Average | Average value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default 0. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1078 | R/W | 8 | Excitation Data Average | Average value for each of 4 excitation channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default 0. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |

To set the average weight, write 0 to 15 to the module registers at addresses 120-127. Note that this address block is offset by 2000 * R. Once an Average Weight selection is made it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 4. Set the Average Weight of Channel 2 to a value of 4. Assume an internal sample rate of 4kS/s and 24-bit data, and read the following parameters for Channel 2: Minimum Data, Maximum Data, and Average Data.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 4 = 8000

Write to system register address 8000+122 = 8122 a data value of 4 to set Signal Data Average Weight
Write to system register address 8000+126 = 8126 a data value of 4 to set Excitation Data Average Weight

Read from system register address 8000+1034 = 9034 the Channel 2 signal minimum data LSB
Read from system register address 8000+1035 = 9035 the Channel 2 signal minimum data MSB

Read from system register address 8000+1054 = 9054 the Channel 2 signal maximum data LSB
Read from system register address 8000+1055 = 9055 the Channel 2 signal maximum data MSB

Note that minimum and maximum data is not stored for the excitation.

Read from system register address 8000+1074 = 9074 the Channel 2 signal average data LSB
Read from system register address 8000+1075 = 9075 the Channel 2 signal average data MSB

Read from system register address 8000+1082 = 9082 the Channel 2 excitation average data LSB
Read from system register address 8000+1083 = 9083 the Channel 2 excitation average data MSB

## 23.0 V/V Ratiometric Signal Representation

Many strain gage signal conditioners use a four-wire connection to the bridge to simplify field wiring. Four wire connections require the excitation voltage source to be accurate and stable over temperature, time, and load. They also require short connections between the strain gage and signal conditioner to reduce errors caused by voltage drops across wiring resistance. One method to reduce these errors is outlined in the *Remote Sense* section of this manual. Another method to eliminate these errors is ratiometric signal representation. Because a Wheatstone bridge output is directly related to the bridge excitation voltage, by using a ratiometric measurement, variations in bridge output due to excitation changes over time, temperature, load, or leadwire resistance cancel out.

The MAQ20-BRDG1 module offers the option to return measured data in ratiometric format, or V/V representation. When this option is selected, data is presented as:

V/V = Measured Voltage Input Signal / Measured Voltage Excitation

This measurement is dimensionless and is a 32-bit floating point number.

V/V ratiometric measurement is calculated and stored in a separate set of module registers during standard operation as outlined in the *Continuous Scan Mode* section of this manual. This data can be retrieved at any time by accessing these module registers. Additionally, V/V can be selectively applied to measured data captured in short time periods as outlined in the *Burst Scan Mode* section of this manual. This selection is made by writing a code to a module register.

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. V/V measurements are stored starting at module register address 1020, which is system register address 2000 * R + 1020, where R is the module Registration Number. V/V Enable is stored at module register address 1097, which is system register address 2000 * R + 1097. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1020 | R/W | 8 | V/V output | 4 channels V/V reading. Integer part at 1xxx, fractional part at 1xxx+1. | -0.04 to +0.04 | Float32 |
| 1097 | R/W | 1 | V/V Calculation Enable | Burst Scan Mode Only 1 = Enabled 0 = Disabled Default = 0 | 0 or 1 | INT16 |
| 1110 | R | 100 | Read Data Buffer | Burst Scan Mode Only Used for data transfer from internal memory. INT32: 24-bit data LSB at 1xxx, MSB at 1xxx+1. INT16:16-bit data at 1xxx. Float32: Integer part at 1xxx, fractional part at 1xxx+1. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 or -0.10 to +0.10 | INT32 / INT16 / Float32 |

To enable V/V calculation for burst scan mode, write 1 to module register address 1097. Note that this address block is offset by 2000 * R. Once burst scan configuration is chosen, it can be saved to local memory by writing a 0 to module register 119.

*Example: A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 4. Enable V/V calculation for burst scan mode and retrieve ratiometric data for continuous scan and burst scan acquisitions.*

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 4 = 8000

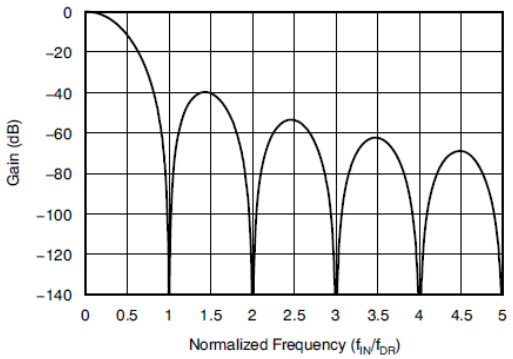
Write to system register address 8000+1097 = 9097 a data value of 1 to enable V/V calculation for burst scan

Read from system register address 8000+1020 to 1027 = 9020 to 9027 the Channel 0 to Channel 3 ratiometric measurements. Data retrieved will be in Float32 format with integer part at module register 1xxx and fractional part at module register 1xxx+1.

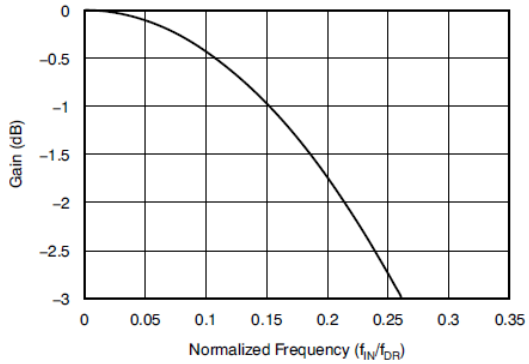
Configure a burst scan and retrieve the collected data by following the instructions outlined in the *Burst Scan Mode* section of this manual. Data retrieved will be in Float32 format with integer part at module register 1xxx and fractional part at module register 1xxx+1.

## 24.0 FIR (Finite Impulse Response) Filter

The MAQ20-BRDG1 module has an internal signal filter which scales with the internal sampling rate chosen. To set sample rate, refer to the *Signal Sample Rate* of this manual. This filter has notches or zeros at multiples of the sample rate.

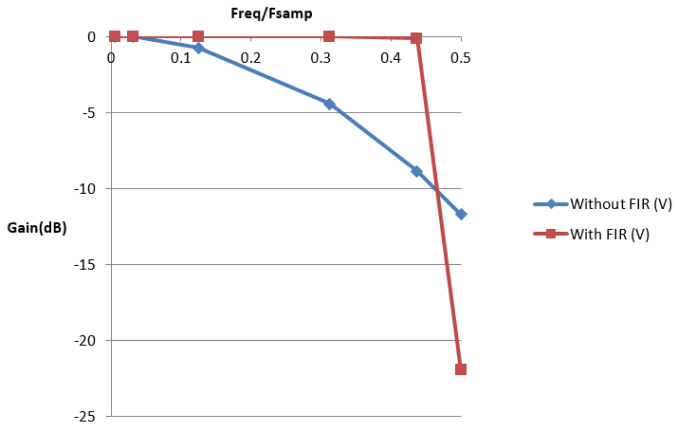



Signal attenuation follows this characteristic.




The MAQ20-BRDG1 module offers the option to use an FIR filter to increase the signal bandwidth. This option is not available in continuous scan mode. The FIR filter can be selectively applied to measured data captured in short time periods as outlined in the *Burst Scan Mode* section of this manual. This selection is made by writing a code to a module register.

When the FIR filter is enabled, signal filter passband attenuation is reduced to produce a flat characteristic up to 40% of the sampling rate.




The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. FIR Filter Enable is stored at module register address 1096, which is system register address 2000 * R + 1096, where R is the module Registration Number. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1096 | R/W | 1 | FIR filter Enable | Burst Scan Mode Only<br>1 = Enabled, 0 = Disabled<br>Default = 0 | 0 or 1 | INT16 |
| 1110 | R | 100 | Read Data Buffer | Burst Scan Mode Only<br>Used for data transfer from internal memory.<br>INT32: 24-bit data LSB at 1xxx, MSB at 1xxx+1.<br>INT16:16-bit data at 1xxx.<br>Float32: Integer part at 1xxx, fractional part at 1xxx+1. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 or -0.10 to +0.10 | INT32 / INT16 / Float32 |

To enable FIR filter for burst scan mode, write 1 to module register address 1096. Note that this address block is offset by 2000 * R. Once FIR filter configuration is chosen, it can be saved to local memory by writing a 0 to module register 119.

*Example:* A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 4. Enable FIR filter for burst scan mode and retrieve data from a burst scan acquisition.

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 4 = 8000

Write to system register address 8000+1097 = 9096 a data value of 1 to enable FIR filter for burst scan

Configure a burst scan and retrieve the collected data by following the instructions outlined in the *Burst Scan Mode* section of this manual. The data retrieved will have the filter compensation applied.

## 25.0 Alarm Functions

Alarms in the MAQ20-BRDG1 module can be set for input signal or V/V measurements acquired in continuous scan mode. Alarms have the following parameters which can be set to meet application requirements.

**Alarm Enable**

Enables the Alarm on a given channel provided that the Alarm Configuration register has a valid configuration. Set the bit corresponding to the given channel to a 1 to enable the alarm. If the Alarm Configuration register for the given channel does not have a valid value, the write will be ignored and the Alarm Enable bit will remain 0. Write a 0 to the bit corresponding to the given channel to disable the alarm and clear any alarms that have tripped.

**Alarm Configuration**

Selects Tracking or Latching alarms for a given channel and selects which limits trip the alarm - High, Low, High-High or Low-Low. There is a module register for each channel. The value written to this module register is the sum of the codes for the Alarm Type and Alarm Limits. Refer to the *Setting and Monitoring Alarms* section of this manual for the specific codes. If an invalid value is written to this module register, the value will be ignored and the last valid value that the module register contained will be kept. If a 0 is written to the module register, the Alarm Enable module register for the channel will be set to 0 and alarms that the channel has tripped will be cleared.

Tracking alarms follow the value of the input signal and reset automatically when the signal comes back into the valid range specified by the limit and deadband. Latching alarms trip when the signal exceeds the alarm condition and remains set until reset by the user.

**High Limit**

Sets the value for the High limit in counts. Alarm status is stored in a module register.

**Low Limit**

Sets the value for the Low limit in counts. Alarm status is stored in a module register.

**High Low Deadband**

Used for the High and/or Low limits to prevent false tripping or alarm chatter for noisy signals. Deadband is the region less than the High limit or greater than the Low limit, measured in counts, which the signal must traverse through before the alarm is reset after being tripped.

**High-High Limit**

Sets the value for the High-High limit in counts. Alarm status is stored in a module register.

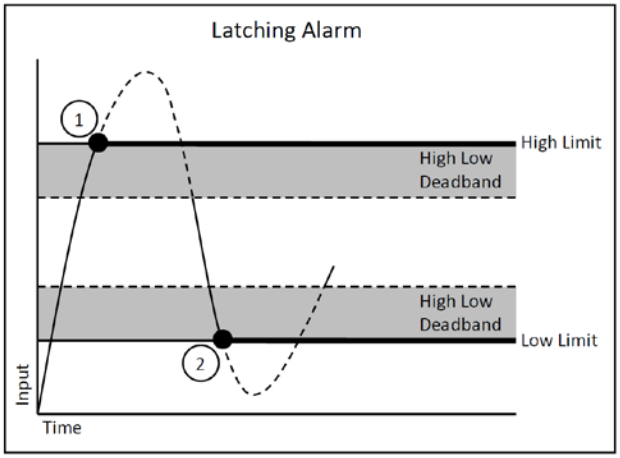
**Low-Low Limit**

Sets the value for the Low-Low limit in counts. Alarm status is stored in a module register.

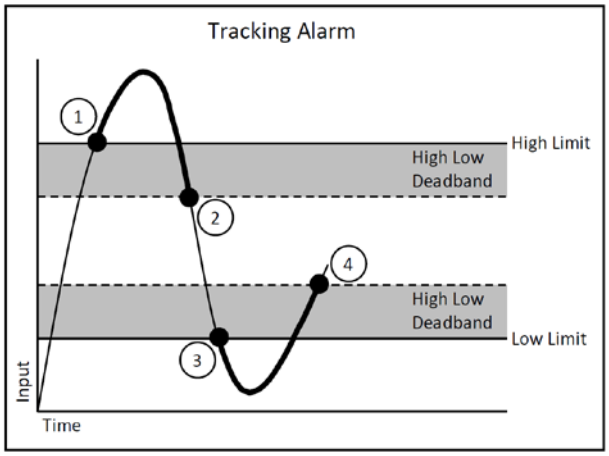
**High-High Low-Low Deadband**

Used for the High-High and/or Low-Low limits to prevent false tripping or alarm chatter for noisy signals. Deadband is the region less than the High-High limit or greater than the Low-Low limit, measured in counts, which the signal must traverse through before the alarm is reset after being tripped.

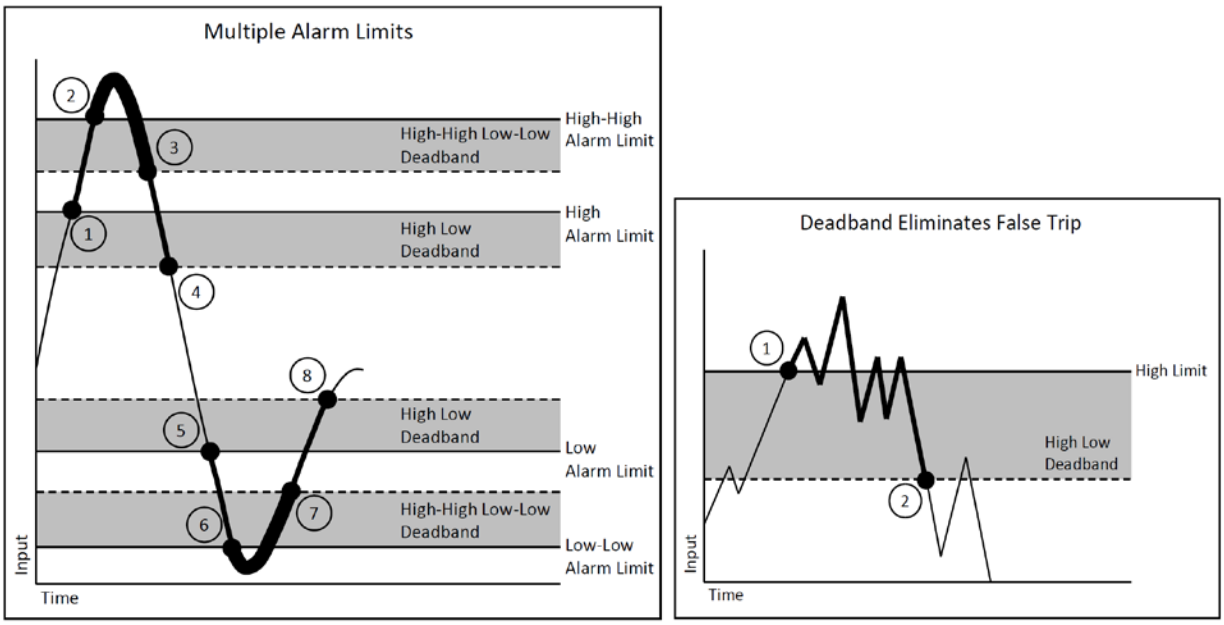
See Figure 20 below for graphical representations of alarm parameters and functionality.




1. High Alarm Tripped
2. Low Alarm Tripped




1. High Alarm Tripped
2. High Alarm Reset
3. Low Alarm Tripped
4. Low Alarm Reset




1. High Alarm Trip
2. High-High Alarm Trip
3. High-High Alarm Reset
4. High Alarm Reset
5. Low Alarm trip
6. Low-Low Alarm Trip
7. Low-Low Alarm Reset
8. Low Alarm Reset

1. High Alarm Trip
2. High Alarm Reset

**Figure 20: Alarm Parameters and Functionality**

## 26.0 Setting and Monitoring Alarms

Alarm settings can be individually set for each signal input channel. Alarm type and limit type are set by writing a value to a module configuration register which is the sum of a number representing the type of alarm and a number representing the alarm limits to be monitored. Alarms are enabled and disabled by writing a 1 or 0 to a module enable register. Alarm Status is stored in a module register block next to the module configuration registers and is mirrored to a module register block next to the input channel readings. When an alarm condition occurs, the appropriate module status register is updated and the red LED on the top panel of the module will light. The module status registers can be monitored by host software for alarm detection. In addition, the MAQ20-BRDG1 module has the ability to map alarm events to other actions with the system.

**Alarm Configuration Value = Alarm Type Code + Alarm Limit Code**

| Alarm Type | Code |
|---|---|
| Tracking | 1000 |
| Latching | 2000 |

| Alarm Limit | Code |
|---|---|
| Low Limit | 100 |
| High Limit | 200 |
| High Low Limits | 300 |
| Low-Low Limit | 400 |
| High-High Limit | 500 |
| High-High Low-Low Limits | 600 |

The *MAQ20-BRDG1 Address Map* is found at the end of this manual. An excerpt from the Address Map is shown below. Alarm status registers and configuration parameters are stored starting at module register address 700, which is system register address 2000 * R + 700, where R is the module Registration Number. Alarm status registers are repeated starting at module register address 1016, which is system register address 2000 * R + 1016. Refer to the *MAQ20 I/O Module Registration* section for further details on Registration Number.

| Address Range 700 - 999: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read / Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 700 | R/W | 1 | Alarm Status, Low-Low Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit.<br>Default = 0. | 0 to 15 | INT16 |
| 701 | R/W | 1 | Alarm Status, Low Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit.<br>Default = 0. | 0 to 15 | INT16 |
| 702 | R/W | 1 | Alarm Status, High Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit.<br>Default = 0. | 0 to 15 | INT16 |
| 703 | R/W | 1 | Alarm Status, High-High Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit.<br>Default = 0. | 0 to 15 | INT16 |
| 704 | R/W | 1 | Alarm Enable | 1 = Enabled 0 = Disabled<br>Default = 0 | 0 to 2600 | INT16 |
| 709 | W | 1 | Save Alarm Parameters to Local Memory | Writing 1 will save the Alarm Configuration, High Limit, Low Limit, High-Low Deadband, High-High Limit, Low-Low Limit and High-High Low-Low Deadband. | | |
| 710 | R/W | 4 | Alarm Configuration | Alarm Configuration<br>Default = 0 | 0 to 2600 | INT16 |
| 730 | R/W | 8 | High Limit | High Alarm Limit. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = +f.s. | 0 to $2^{32}$-1 | INT32 |
| 750 | R/W | 8 | Low Limit | Low Alarm Limit. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = -f.s. | 0 to $2^{32}$-1 | INT32 |
| 770 | R/W | 8 | High Low Deadband | Deadband for High Low Alarm. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = 0. | 0 to $2^{32}$-1 | INT32 |
| 790 | R/W | 8 | High-High Limit | High-High Alarm Limit. 24-bit data LSB at xxx, MSB at xxx+1. 16-bit data at xxx. Default = +f.s. | 0 to $2^{32}$-1 | INT32 |
| 810 | R/W | 8 | Low-Low Limit | Low-Low Alarm Limit. 24-bit data LSB at 8xx, MSB at 8xx+1. 16-bit data at 8xx. Default = -f.s. | 0 to $2^{32}$-1 | INT32 |
| 830 | R/W | 8 | High-High Low-Low Deadband | Deadband for High-High Low-Low Alarm. 24-bit data LSB at 8xx, MSB at 8xx+1. 16-bit data at 8xx. Default = 0. | 0 to $2^{32}$-1 | INT32 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read / Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1016 | R | 1 | Alarm Status, Low-Low Bitwise | Status of Low-Low Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1017 | R | 1 | Alarm Status, Low Bitwise | Status of Low Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1018 | R | 1 | Alarm Status, High Bitwise | Status of High Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1019 | R | 1 | Alarm Status, High-High Bitwise | Status of High-High Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |

Once alarm configuration is complete it can be saved to local memory by writing a 1 to module register 709. If the alarm configuration value is 0, the alarm is off (disabled). The alarm for a given channel cannot be turned on (enabled) until a valid, non-zero value is written to the module alarm configuration register.

*Example:* A MAQ20-BRDG1 module with serial number 1234567-89 is installed in a system and has been assigned a Registration Number of 3. Set up the module to have a Tracking Alarm on Channel 1 with a High limit of 4170000 counts, a Low limit of 200000 counts and a Deadband of 10000 counts.

The MAQ20-BRDG1 module with s/n 1234567-89 has an address offset of 2000 * 3 = 6000

Write to system register address 6000+711 = 6711 a value of 2000+300 = 2300 to set a Latching Alarm with High Low limit on Channel 1

Write to system register address 6000+731 = 6731 a value of 4170000 to set the High limit on Channel 1

Write to system register address 6000+751 = 6751 a value of 200000 to set the Low limit on Channel 1

Write to system register address 6000+771 = 6711 a data value of 10000 to set the Deadband for the High and Low limits on Channel 1

Write to system register address 6000+704 = 6704 the equivalent of bit code 0000 0010 = 2 to enable the alarm on Channel 1

Write to system register address 6000+709 = 6709 a data value of 1 to save the configuration to memory

When an alarm condition is reached as specified by the above parameters, the module Alarm Status registers are updated in response to the events and the red LED on the module is lit.

Read system register address 6000+701 = 6701 to view the status of the Low Alarm.
If bit code 0000 0010 = 3 is read, the low alarm limit plus deadband was exceeded on Channel 1

Write to system register address 6000+701 = 6701 the equivalent of bit code 0000 0000 = 0 to clear the Channel 1 latched alarm. The red LED will be turned off.

Read system register address 6000+702 = 6702 to view the status of the High Alarm.
If bit code 0000 0010 = 3 is read, the high alarm limit plus deadband was exceeded on Channel 1

## 27.0 Reset Functions

Two types of firmware reset are supported in the MAQ20 I/O modules:

***Standard Reset*** is used to put the module in a user-defined state. The parameters listed below will be set to the last state saved to local memory. User parameters stored in local memory are not affected and will be reloaded upon power cycle. If the parameters listed below are to be changed and saved to local memory, make the changes then perform a Save to Local Memory operation.

***Reset-to-Default*** reverts the module to the settings used at the factory during manufacture. It performs the standard reset actions plus resets non-volatile parameters to default settings. User parameters stored in local memory are not affected and will be reloaded upon power cycle. To return a module to original factory configuration, perform a Reset-to-Default followed by a Save to Local Memory operation.

The table below shows which parameters are affected for each reset.

**Table 3: Parameters Affected by Standard Reset and Reset-to-Default**

| RESET TYPE | PARAMETERS |
|---|---|
| Standard Reset | Disables all Alarms, Clears Alarm Status<br><br>Resets module Min, Max and Average registers to 0<br><br>Resets Signal Gain, Average Weight, Excitation Voltage, Bridge Configuration, Shunt Calibration, Auto Zero, Sampling Rate, FIR Filter Enable, V/V Calculation Enable, Burst Sample Count, Burst Channel Enable to values set in Local Memory<br><br>Clears all module Status and Diagnostic registers |
| Reset-to-Default | All parameters listed under Standard Reset, plus:<br><br>Resets Signal Gain, Average Weight, Excitation Voltage, Bridge Configuration, Shunt Calibration, Auto Zero, Sampling Rate, FIR Filter Enable, V/V Calculation Enable, Burst Sample Count, Burst Channel Enable to values to factory default values<br><br>Clears all Alarm Limits and Deadbands |

**Reset Registers**

Writing a valid data value to the module Reset Register will force the module to perform a specified reset. Write 0 to perform Standard Reset or write 255 to perform Reset-to-Default.

NOTE: The MAQ20 I/O modules send a response to the reset register write before carrying out the reset. This means the module will be unresponsive to commands for approximately 3 seconds.

**Power-On-Reset (POR)**

MAQ20 I/O modules utilize a watchdog timer to ensure reliable and predictable operation under all conditions. Upon power cycle or any extreme circumstance under which the watchdog timer expires, a Standard Reset is performed, and parameters stored in local memory are loaded to the appropriate module registers.

## 28.0 MAQ20-BRDG1 Address Map

The table in this section outlines the MAQ20-BRDG1 address space. Data in these registers contains all permanent and user settable information for module configuration, status, operation of all functions, data read/write, and data storage. Table columns list the following information:

**Start Address:** Start address for the specified quantity of addresses. The start address is offset by 2000 * R where R is the module Registration Number.

**Read/Write:** Indicates whether data at the address is Read, Write or both.

**Number of Registers:** The number of 16-bit registers reserved for the specified contents.

**Contents:** Parameter stored at the specified address.

**Description:** Details, examples, limits, and default values for the parameter stored at the specified address.

**Data Range:** Valid data read from or written to an address range. Data not in this range which is written to an address may return a Modus Exception 3, Illegal Data, or may be ignored.

**Data Type:** The type of data stored at the specified address.

**ASCII** 0123456789ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz, -, “ “
**INT16** 16-bit integer value, 0 to 65535, unless otherwise indicated. Stored at a single address.
**INT32** 32-bit integer value, 0 to 4294967295, unless otherwise indicated. Stored at two 16-bit addresses. MSB is stored at address N, LSB is stored at address N+1.

Module register addresses 0 to 1999 in the table below are system register addresses 2000 * R + 0 to 1999, where R is the module Registration Number. Refer to the MAQ20 I/O Module Registration section for further details on Registration Number.

**Table 4: MAQ20-BRDG1 Address Map**

| Address Range 0 - 99: Module Information | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 0 | R | 15 | Device Description | MAQ20-BRDG1 | Characters, Numbers, "-" and Space | ASCII |
| 19 | R | 11 | Serial Number | S1234567-89 | Characters, Numbers, "-" and Space | ASCII |
| 30 | R | 5 | Date Code | D0915 (D<week><year>) | Characters, Numbers | ASCII |
| 35 | R | 5 | Firmware Rev | F1.00 | Characters, 0-9 and "." | ASCII |
| 40 | R | 1 | Input Channels | 8 Input Channels | 8 | ASCII |
| 41 | R | 1 | Output Channels | 0 Output Channels | 0 | ASCII |
| 98 | W | 1 | Module Detect | Any write will blink Status LED at 5Hz for 5 seconds | 0 to 65,535 | INT16 |
| 99 | W | 1 | Reset Register | 0 = Standard Reset, 255 = Reset to Default | 0, 255 | INT16 |

| Address Range 100 - 699: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 100 | R/W | 4 | Input Range | 0 = ±100mV (Default)<br>1 = ±50mV<br>2 = ±25mV<br>3 = ±12.5mV<br>4 = ±8.33mV | 0 to 4 | INT16 |
| 119 | W | 1 | Save to Local Memory | Writing 0 will save Signal Gain, Average Weight, $V_{exc}$, Half Bridge, Shunt Calibration, Auto Zero, Sampling Rate. | | INT16 |
| 120 | R/W | 8 | Average Weight | Weight for Average Calculation. Default = 0. | 0 to 15 | INT16 |
| 600 | R/W | 1 | Excitation Voltage | 0 = 2.5V, 1 = 3.3V, 2 = 5V, 3 = 10V. Default = 0. | 0 to 3 | INT16 |
| 610 | R/W | 4 | Bridge Configuration | 0 = Half Bridge, 1 = Full Bridge. Default = 1. | 0 or 1 | INT16 |
| 620 | R/W | 4 | Shunt Calibration Resistors | 0 = 60kohm, 1 = 100kohm, 2 = 200kohm and 3 = External. Default = 0. | 0 to 3 | INT16 |
| 624 | R/W | 1 | Shunt Calibration On/Off | 0 = On, 1 = Off. Default = 1. | 0 or 1 | INT16 |
| 626 | R/W | 1 | Auto Zero Ch 0 Enable | 1 = Set new zero value, 0 = Clear zero. Default = 0. | 0 or 1 | INT16 |
| 627 | R/W | 1 | Auto Zero Ch 1 Enable | 1 = Set new zero value, 0 = Clear zero. Default = 0. | 0 or 1 | INT16 |
| 628 | R/W | 1 | Auto Zero Ch 2 Enable | 1 = Set new zero value, 0 = Clear zero. Default = 0. | 0 or 1 | INT16 |
| 629 | R/W | 1 | Auto Zero Ch 3 Enable | 1 = Set new zero value, 0 = Clear zero. Default = 0. | 0 or 1 | INT16 |
| 630 | R/W | 8 | Auto Zero Values | 4 channel Auto Zero values. 24-bit data LSB at 63x, MSB at 63x+1. 16-bit data at 63x. | | INT32 / INT16 |
| 678 | R/W | 1 | Sampling Rate & Resolution | 0 = future use<br>1 = 16bit, 32kS/s<br>2 = 24bit, 16kS/s<br>3 = 24bit, 8kS/s<br>4 = 24bit, 4kS/s (Default)<br>5 = 24bit, 2kS/s<br>6 = 24bit, 1kS/s | 1 to 6 | INT16 |

| Address Range 700 - 999: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 700 | R/W | 1 | Alarm Status, Low-Low Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit. Default = 0. | 0 to 15 | INT16 |
| 701 | R/W | 1 | Alarm Status, Low Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit. Default = 0. | 0 to 15 | INT16 |
| 702 | R/W | 1 | Alarm Status, High Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit. Default = 0. | 0 to 15 | INT16 |
| 703 | R/W | 1 | Alarm Status, High-High Bitwise | 0 = No Alarm<br>1 = Alarm Limit Exceeded<br>To clear a Latched alarm, write a 0 to the corresponding channel bit. Default = 0. | 0 to 15 | INT16 |
| 704 | R/W | 1 | Alarm Enable | 1 = Enabled 0 = Disabled<br>Default = 0 | 0 to 2600 | INT16 |
| 709 | W | 1 | Save Alarm Parameters to Local Memory | Writing 1 will save the Alarm Configuration, High Limit, Low Limit, High-Low Deadband, High-High Limit, Low-Low Limit and High-High Low-Low Deadband. | | |
| 710 | R/W | 4 | Alarm Configuration | Alarm Configuration<br>Default = 0 | 0 to 2600 | INT16 |
| 730 | R/W | 8 | High Limit | High Alarm Limit. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = +f.s. | 0 to $2^{32}$-1 | INT32 |
| 750 | R/W | 8 | Low Limit | Low Alarm Limit. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = -f.s. | 0 to $2^{32}$-1 | INT32 |

| Address Range 700 - 999: Module Configuration | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 770 | R/W | 8 | High Low Deadband | Deadband for High Low Alarm. 24-bit data LSB at 7xx, MSB at 7xx+1. 16-bit data at 7xx. Default = 0. | 0 to $2^{32}$-1 | INT32 |
| 790 | R/W | 8 | High-High Limit | High-High Alarm Limit. 24-bit data LSB at xxx, MSB at xxx+1. 16-bit data at xxx. Default = +f.s. | 0 to $2^{32}$-1 | INT32 |
| 810 | R/W | 8 | Low-Low Limit | Low-Low Alarm Limit. 24-bit data LSB at 8xx, MSB at 8xx+1. 16-bit data at 8xx. Default = -f.s. | 0 to $2^{32}$-1 | INT32 |
| 830 | R/W | 8 | High-High Low-Low Deadband | Deadband for High-High Low-Low Alarm. 24-bit data LSB at 8xx, MSB at 8xx+1. 16-bit data at 8xx. Default = 0. | 0 to $2^{32}$-1 | INT32 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1000 | R | 8 | Channel Data | Data for 4 Signal Channels. 24-bit data LSB at 100x, MSB at 100x+1. 16-bit data at 100x, 100x+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1008 | R | 8 | EXC Data | Data for 4 Excitation Channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx, 10xx+2. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1016 | R | 1 | Alarm Status, Low-Low Bitwise | Status of Low-Low Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1017 | R | 1 | Alarm Status, Low Bitwise | Status of Low Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1018 | R | 1 | Alarm Status, High Bitwise | Status of High Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1019 | R | 1 | Alarm Status, High-High Bitwise | Status of High-High Alarm<br>0 = No Alarm<br>1 = Alarm Limit Exceeded<br>Default = 0 | 0 to 15 | INT16 |
| 1020 | R/W | 8 | V/V output | 4 channels V/V reading. Integer part at 1xxx, fractional part at 1xxx+1. | -0.04 to +0.04 | Float32 |
| 1030 | R/W | 8 | Signal Data Minimum | Minimum value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = -f.s. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1030 | R/W | 8 | Signal Data Minimum | Minimum value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = -f.s. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1050 | R/W | 8 | Signal Data Maximum | Maximum value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = +f.s. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1070 | R/W | 8 | Signal Data Average | Average value for each of 4 signal channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = 0. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |

| Address Range 1000 - 1699: Module Data | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Contents** | **Description** | **Data Range** | **Data type** |
| 1078 | R/W | 8 | Excitation Data Average | Average value for each of 4 excitation channels. 24-bit data LSB at 10xx, MSB at 10xx+1. 16-bit data at 10xx. Default = 0. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 | INT32 / INT16 |
| 1096 | R/W | 1 | FIR filter Enable | Burst Scan Mode Only<br>1 = Enabled, 0 = Disabled<br>Default = 0 | 0 or 1 | INT16 |
| 1097 | R/W | 1 | V/V Calculation Enable | Burst Scan Mode Only<br>1 = Enabled 0 = Disabled<br>Default = 0 | 0 or 1 | INT16 |
| 1098 | R/W | 2 | Number of Samples to Read | Burst Scan Mode Only 24-bit data, 2M sample max. 16-bit data, 4M sample max. LSB at 1098, MSB at 1099.<br>Default = 1000000 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1100 | R/W | 1 | Scan Start | Burst Scan Mode Only<br>1 = Start, 0 = Stop<br>Default = 0 | 0 or 1 | INT16 |
| 1101 | R/W | 4 | Channel Enable | Burst Scan Mode Only<br>Channels to be included in Burst Scan<br>1 = Enable, 0 = Disable<br>Default = 0 | 0 or 1 | INT16 |
| 1105 | R | 2 | Available Storage | Burst Scan Mode Only<br>Storage space remaining, expressed in number of samples. 24-bit data, 2M sample max. 16-bit data 4M sample max. LSB at 1105, MSB at 1106.<br>Default = 2000000 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1107 | R/W | 2 | Read Counter | Burst Scan Mode Only<br>Sample read counter. 24-bit data, 2M sample max. 16-bit data 4M sample max. LSB at 1107, MSB at 1108.<br>Default = 0 | 24-bit data 0 to 2000000, 16-bit data 0 to 4000000 | INT32 |
| 1110 | R | 100 | Read Data Buffer | Burst Scan Mode Only<br>Used for data transfer from internal memory.<br>INT32: 24-bit data LSB at 1xxx, MSB at 1xxx+1.<br>INT16:16-bit data at 1xxx.<br>Float32: Integer part at 1xxx, fractional part at 1xxx+1. | 0 to $2^{32}$-1 or 0 to $2^{16}$-1 or -0.10 to +0.10 | INT32 / INT16 / Float32 |

| Address Range 1700 - 1899: Input Ranges |
|---|

| Start Address | Read/Write | Number of Registers | Contents | Description | Data Range | Data type |
|---|---|---|---|---|---|---|
| **1700** | **R** | **1** | **Range Count** | **Number of ranges supported** | **1 to 5** | **INT16** |
| **1710** | **R** | **1** | **Range 0** | **Engineering -fs.** | **-32,768 to 32,767** | **INT16** |
| 1711 | R | 1 | Range 0 | Future Use | -32,768 to 32,767 | INT16 |
| 1712 | R | 1 | Range 0 | Engineering +fs | -32,768 to 32,767 | INT16 |
| 1713 | R | 1 | Range 0 | Future Use | -32,768 to 32,767 | INT16 |
| 1714 | R | 1 | Range 0 | +fs & -fs multiplier Factor $10^X$ | -32,768 to 32,767 | INT16 |
| 1715 | R | 1 | Range 0 | Engineering Units ("C", "V", etc) | A to Z | ASCII |
| 1716 | R | 1 | Range 0 | Engineering Units ("C", "V", etc) | A to Z | ASCII |
| 1717 | R | 1 | Range 0 | Future Use | -32,768 to 32,767 | INT16 |
| 1718 | R | 1 | Range 0 | Count Value of -fs. | -32,768 to 32,767 | INT16 |
| 1719 | R | 1 | Range 0 | Future Use | -32,768 to 32,767 | INT16 |
| 1720 | R | 1 | Range 0 | Count Value of +fs. | -32,768 to 32,767 | INT16 |
| **1730** | **R** | **1** | **Range 1** | **Engineering -fs.** | **-32,768 to 32,767** | **INT16** |
| 1731 | R | 1 | Range 1 | Future Use | -32,768 to 32,767 | INT16 |
| 1732 | R | 1 | Range 1 | Engineering +fs | -32,768 to 32,767 | INT16 |
| 1733 | R | 1 | Range 1 | Future Use | -32,768 to 32,767 | INT16 |
| 1734 | R | 1 | Range 1 | +fs & -fs multiplier Factor $10^X$ | -32,768 to 32,767 | INT16 |
| 1735 | R | 1 | Range 1 | Engineering Units ("C", "V", etc) | A to Z | ASCII |
| 1736 | R | 1 | Range 1 | Engineering Units ("C", "V", etc) | A to Z | ASCII |
| 1737 | R | 1 | Range 1 | Future Use | -32,768 to 32,767 | INT16 |
| 1738 | R | 1 | Range 1 | Count Value of -fs. | -32,768 to 32,767 | INT16 |
| 1739 | R | 1 | Range 1 | Future Use | -32,768 to 32,767 | INT16 |
| 1740 | R | 1 | Range 1 | Count Value of +fs. | -32,768 to 32,767 | INT16 |

**Address Range 1700 - 1899: Input Ranges**

| Start Address | Read/Write | Number of Registers | Contents | Description | Data Range | Data type |
|---|---|---|---|---|---|---|
| **1750** | **R** | **1** | **Range 2** | **Engineering -fs.** | **-32,768 to 32,767** | **INT16** |
| 1751 | R | 1 | Range 2 | Future Use | -32,768 to 32,767 | INT16 |
| 1752 | R | 1 | Range 2 | Engineering +fs | -32,768 to 32,767 | INT16 |
| 1753 | R | 1 | Range 2 | Future Use | -32,768 to 32,767 | INT16 |
| 1754 | R | 1 | Range 2 | +fs & -fs multiplier Factor $10^X$ | -32,768 to 32,767 | INT16 |
| 1755 | R | 1 | Range 2 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1756 | R | 1 | Range 2 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1757 | R | 1 | Range 2 | Future Use | -32,768 to 32,767 | INT16 |
| 1758 | R | 1 | Range 2 | Count Value of -fs. | -32,768 to 32,767 | INT16 |
| 1759 | R | 1 | Range 2 | Future Use | -32,768 to 32,767 | INT16 |
| 1760 | R | 1 | Range 2 | Count Value of +fs. | -32,768 to 32,767 | INT16 |
| **1770** | **R** | **1** | **Range 3** | **Engineering -fs.** | **-32,768 to 32,767** | **INT16** |
| 1771 | R | 1 | Range 3 | Future Use | -32,768 to 32,767 | INT16 |
| 1772 | R | 1 | Range 3 | Engineering +fs | -32,768 to 32,767 | INT16 |
| 1773 | R | 1 | Range 3 | Future Use | -32,768 to 32,767 | INT16 |
| 1774 | R | 1 | Range 3 | +fs & -fs multiplier Factor $10^X$ | -32,768 to 32,767 | INT16 |
| 1775 | R | 1 | Range 3 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1776 | R | 1 | Range 3 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1777 | R | 1 | Range 3 | Future Use | -32,768 to 32,767 | INT16 |
| 1778 | R | 1 | Range 3 | Count Value of -fs. | -32,768 to 32,767 | INT16 |
| 1779 | R | 1 | Range 3 | Future Use | -32,768 to 32,767 | INT16 |
| 1780 | R | 1 | Range 3 | Count Value of +fs. | -32,768 to 32,767 | INT16 |

**Address Range 1700 - 1899: Input Ranges**

| Start Address | Read/Write | Number of Registers | Contents | Description | Data Range | Data type |
|---|---|---|---|---|---|---|
| **1790** | **R** | **1** | **Range 4** | **Engineering -fs.** | **-32,768 to 32,767** | **INT16** |
| 1791 | R | 1 | Range 4 | Future Use | -32,768 to 32,767 | INT16 |
| 1792 | R | 1 | Range 4 | Engineering +fs | -32,768 to 32,767 | INT16 |
| 1793 | R | 1 | Range 4 | Future Use | -32,768 to 32,767 | INT16 |
| 1794 | R | 1 | Range 4 | +fs & -fs multiplier Factor $10^X$ | -32,768 to 32,767 | INT16 |
| 1795 | R | 1 | Range 4 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1796 | R | 1 | Range 4 | Engineering Units ("C", "V", etc.) | A to Z | ASCII |
| 1797 | R | 1 | Range 4 | Future Use | -32,768 to 32,767 | INT16 |
| 1798 | R | 1 | Range 4 | Count Value of -fs. | -32,768 to 32,767 | INT16 |
| 1799 | R | 1 | Range 4 | Future Use | -32,768 to 32,767 | INT16 |
| 1800 | R | 1 | Range 4 | Count Value of +fs. | -32,768 to 32,767 | INT16 |

| **Address Range 1900 - 1999: Status Registers** | | | | | | |
|---|---|---|---|---|---|---|
| **Start Address** | **Read/Write** | **Number of Registers** | **Type** | **Example** | **Range** | **Data type** |
| 1900 | R/W | 1 | Watchdog Reset | 0 = Normal<br>1 = Watchdog Reset Occurred | 0 or 1 | INT16 |
| 1902 | R/W | 1 | I2C Error | I2C TX Error Counter | 0 to 65,535 | INT16 |
| 1903 | R/W | 1 | I2C Error | I2C RX Error Counter | 0 to 65,535 | INT16 |
| 1906 | R/W | 1 | Numeric Error | Increments when a value received is outside of the allowed range.<br>Default = 0. | 0 to 65,535 | INT16 |
| 1908 | R/W | 1 | UART RX Error | UART RX Error Counter Command Too Short<br>Default = 0 | 0 to 65,535 | INT16 |
| 1909 | R/W | 1 | UART RX Error | UART RX Error Counter Command Too Long<br>Default = 0 | 0 to 65,535 | INT16 |
| 1910 | R/W | 1 | UART RX Error | UART RX Error Counter Command received in invalid state.<br>Default = 0 | 0 to 65,535 | INT16 |

**Table 5: MAQ20-BRDG1 Range Table**

**Sampling Rate = 1kS/s, 2kS/s, 4kS/s, 8kS/s, 16kS/s**

| | Signal Gain Code | Signal Gain | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|---|
| | 0 (Default) | 1 | -100mV to +100mV | -8197767 to 8197767 | -102.328mV to +102.328mV | -8388608 to 8388607 |
| | 1 | 2 | -50mV to +50mV | -8197767 to 8197767 | -51.164mV to +51.164mV | -8388608 to 8388607 |
| | 2 | 4 | -25mV to +25mV | -8197767 to 8197767 | -25.582mV to +25.582mV | -8388608 to 8388607 |
| | 3 | 8 | -12.5mV to +12.5mV | -8197767 to 8197767 | -12.791mV to +12.791mV | -8388608 to 8388607 |
| | 4 | 12 | -8.33mV to +8.33mV | -8197767 to 8197767 | -8.527mV to +8.527mV | -8388608 to 8388607 |

| | Exc Code | Vexc | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|---|
| **BRDG1** | 0 (Default) | 2.5 | 2.5 | 1310720 | | |
| | 1 | 3.333 | 3.333 | 1747452 | | |
| | 2 | 5 | 5 | 2621440 | | |
| | 3 | 10 | 10 | 5242880 | | |

**Sampling Rate = 32kS/s**

| | Signal Gain Code | Signal Gain | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|---|
| | 0 (Default) | 1 | -100mV to +100mV | -32023 to 32023 | -102.328mV to +102.328mV | -32768 to 32767 |
| | 1 | 2 | -50mV to +50mV | -32023 to 32023 | -51.164mV to +51.164mV | -32768 to 32767 |
| | 2 | 4 | -25mV to +25mV | -32023 to 32023 | -25.582mV to +25.582mV | -32768 to 32767 |
| | 3 | 8 | -12.5mV to +12.5mV | -32023 to 32023 | -12.791mV to +12.791mV | -32768 to 32767 |
| | 4 | 12 | -8.33mV to +8.33mV | -32023 to 32023 | -8.527mV to +8.527mV | -32768 to 32767 |

| | Exc Code | Vexc | Standard Input Voltage | Equivalent Counts | Over/Under Range | Equivalent Counts |
|---|---|---|---|---|---|---|
| **BRDG1** | 0 (Default) | 2.5 | 2.5 | 5120 | | |
| | 1 | 3.333 | 3.333 | 6826 | | |
| | 2 | 5 | 5 | 10240 | | |
| | 3 | 10 | 10 | 20480 | | |

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**MAQ20-BRDG1 Hardware User Manual**
**MA1046 Rev. D – March 2024**

**ISO9001:2015-Registered QMS**